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To: TONIA MEONSKE **Location: RND-2D65** **Art Unit: 2181** **Friday, September 28, 2007** **Case Serial Number: 10/721300**	**From: ALYSON DILL** **Location: EIC2100** **RND-4B28 / RND-4A18** **Phone: (571)272-3527** **alyson.dill@uspto.gov**

Search Notes

Examiner MEONSKE:

A search was executed on the application number listed above. The following database clusters were searched:

- Non-Patent Literature (NPL) abstract files;
- Non-Patent Literature (NPL) fulltext files;
- Patent abstract files;
- Patent fulltext files.

An inventor search was executed. If you require additional information or a refocus of the search contacted:

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Alyson

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File 348:EUROPEAN PATENTS 1978-2007/ 200722
File 349:PCT FULLTEXT 1979-2007/UB=20070531UT=20070525

Set Items Description
S1 926307 SAVE OR SAVING OR SAVED OR STORE OR STORED OR STORING OR K-EEP?
S2 561977 BACKUP? OR BACK??? () UP OR COPY OR COPIES OR COPYING OR -COPIED OR REBUILD? OR REPLACING OR REPLACEMENT? OR RESTORE? ? OR RESTORING OR RESTORED OR UPDATE OR UPDATING OR UPDATED
S3 51390 CLOCK (3N) (CYCLE? OR RATE?? ? OR SPEED? OR PULS??? OR CIR-CUIT?)
S4 1681 S1 (50N) S2 (50N) S3
S5 1679 TWO OR 2 OR MORE OR SOME OR MULTI OR MULTIPLE OR ANOTHER OR DIFFERENT OR OTHER? ? OR ADDITIONAL? OR BOTH OR MANY OR ASSO-RTED OR SEVERAL OR FEW OR SECOND OR DUPLICAT? OR DOUBL? OR DU-AL OR ITERAT? OR PLURAL OR TWIN? ? OR TWINNED
S6 1663 CHANG??? OR CONVERT? OR EXCHANG? OR FLIP OR INTERCHANG??? -OR REPLAC??? OR SUBSTITUT??? OR SWAP??? OR SWITCH??? OR TRANS-FORM???
S7 1666 CHRONOLOGICAL? OR CONSECUTIVE? OR ENSUING OR FOLLOW???? OR SEQUENCE?? ? OR SEQUENTIAL? OR SERIAL? OR SUCCED? OR SUCCESSI?
S8 1282 S5 (5N) S6
S9 369 S8 (15N) S7
S10 369 S4 AND S9
S11 1533 BREAK??? OR DELAY? OR HALT??? OR HESITANCY OR HESITATION? ? OR HOLD??? OR INTERMISSION? ? OR INTERRUPTION? ? OR INTERVA-L? ? OR LAG? ? OR LAGGING OR LAPSE? ? OR LATENC? OR LULL?? OR PAUSE? ?
S12 952 RECESS?? OR RESPITE OR REST? ? OR STALL??? OR SUSPENSION? ? OR WAIT? ? OR WAITING
S13 1582 S11 OR S12
S27 1223 CONSTANT? OR PERMANENT? OR REGULAR? OR STABILE OR STABLE OR STEADFAST OR STEADY OR UNBROKEN OR UNCHANG? OR UNFLUCTUAT? -

OR UNIFORM? OR UNINTERRUPT? OR UNVARY?
S28 287 S13 (5N) S27
S29 106 S10 AND S28
S30 37 (REGISTER? OR MEMORY OR STORE? ? OR STORING OR STORAGE) (-
9N) (ACTIVE OR ACTIVAT??? OR CURRENT??? OR TOP OR FRONT OR F-
OCUS? OR SELECT???)(4W) WINDOW???
S31 18 S29 AND S30
S32 14 S31 AND PY=1963:2002
S33 15 S31 AND AY=1963:2002
S34 15 S32 OR S33
S35 15 S34 AND CLOCK?
S36 15 IDPAT (sorted in duplicate/non-duplicate order)
S37 15 IDPAT (primary/non-duplicate records only)

37/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00996861
Multistandard decoder for Huffman codes

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PATENT (CC, No, Kind, Date): EP 901286 A1 990310 (Basic)
APPLICATION (CC, No, Date): EP 98202135 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
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RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 953013018)
INTERNATIONAL PATENT CLASS (V7): H04N-007/24; G06F-013/00; G06F-009/38;
ABSTRACT WORD COUNT: 155

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 9910 390
SPEC A (English) 9910 126718
Total word count - document A 127108
Total word count - document B 0
Total word count - documents A + B 127108

...SPECIFICATION encoded bit streams arranged as a serial bit stream of digital bits and having separately encoded pairs of start codes and data carried in the serial bit stream, a Start Code Detector subsystem

having first, second and third registers connected in serial fashion, each of the registers storing a different number of bits from the bit stream, the first register storing a value, the second register and...of pipeline stages. Furthermore, data may be processed in more than one stage and the processing time for different stages can differ.

In addition to clock and data signals (described below), the pipeline includes two transfer control signals -- a "VALID" signal and an "ACCEPT" signal. These signals are used to control...3) illustrate generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping clock with phases (o slash)0 and (o slash)1. Although a two-phase clock is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a clock with more than two phases.

As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and...

...the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is snown in Fig. 3. A change of state during a clock phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a ...

...HIGH whenever the storage elements contain valid data.

In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping clock phases (o slash)0 and (o slash)1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during clock cycle (o slash)1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the clock cycle (o slash)0. Fig. 3 also illustrates that the primary and secondary storage elements in each stage are further connected via an internal acceptance...ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective clock phases until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the ol...

37/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00991423
Start code detecting apparatus for video data stream

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APPLICATION (CC, No, Date): EP 98202174 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
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CLAIMS A	(English)	9906	538
SPEC A	(English)	9906	126716

Total word count - document A 127254
Total word count - document B 0
Total word count - documents A + B 127254

...SPECIFICATION initialization of the system, a uniform, prescribed gray scale value or picture half-tone expressed as a defined luminance value is written into the image **store** of a coder at the transmitter and in the image store of a decoder at the receiver store, in the same way for all picture...of the number of components, for a linear-phase filter, and zero-padded to equal the number of samples of a data block, this being **followed** by forming the discrete odd cosine **transform** (DOCT) of the padded kernel matrix.
United States Patent No. 5,175,617 discloses a system and method for transmitting logmap video images through telephone...

...are interleaved for transmission such that the intraframe even field compressed data occurs midway between successive fields of intraframe odd field compressed data. The interleaved **sequence** provides receivers with twice the number of entry points into the signal for decoding without increasing the amount of data transmitted.
United States Patent No...

...the proposed ISO/IEC MPEG standards. Included are three cooperating components or subsystems that operate to variously adaptively pre-process the incoming digital motion video **sequences**, allocate bits to the pictures in a **sequence**, and adaptively quantize **transform** coefficients in **different** regions of a picture in a video **sequence** so as to provide optimal visual quality given the number of bits allocated to that picture.
United States Patent No. 5,267,334 discloses a...

...following the first image in time in the sequence of moving images. This at least one frame being known as an interframe. Finally, detecting a **second** scene **change** in the **sequence** of moving images and generating a second keyframe containing complete scene information for an image displayed at the time ...from a selected number of coefficients along a continuous scan. These sub-blocks may be decoded in a standard fashion, with an inverse discrete cosine **transform** applied to square sub-blocks obtained by the appropriate zero padding of and/or discarding ...block signal in most cases.
United States Patent No. 4,903,018 discloses a process and data

processing system for compressing and expanding structurally associated multiple data sequences. The process is particular to data sets in which an analysis is made of the structure in order to identify a characteristic common to a predetermined number of successive data elements of a data sequence. In place of data elements, a code is used which is again decoded during expansion. The common characteristic is...

...of the number of components, for a linear-phase filter, and zero-padded to equal the number of samples of a data block, this being followed by forming the discrete odd cosine transform (DOCT) of the padded kernel matrix.

United States Patent No. 5,231,486 discloses a high definition video system processes a bitstream including high and...2) illustrate the control of data transfer between stages of a preferred embodiment of a pipeline using a two-wire interface and a multi-phase clock;

Figure. 4 is a block diagram that illustrates a basic embodiment of a pipeline stage that incorporates a two-wire transfer control and also shows...

...in an exemplifying "data duplication" pipeline stage;

Figures. 9a and 9b taken together depict one example of a timing diagram that shows the two-phase clock, the two-wire transfer control signals and the other internal data and control signals used in the exemplifying embodiment shown in Figures. 8a and 8b...

...shows a macroblock structure;

Figure 37 shows a two-wire interface protocol;
Figure 38 shows the location of external two-wire interfaces;
Figure 39 shows clock propagation;
Figure 40 shows two-wire interface timing;
Figure 41 shows examples of access structure;
Figure 42 shows a read transfer cycle;
Figure 43 shows...

...timing;

Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory map;
Figure 56 shows a typical decoder clock regime;
Figure 57 shows input clock requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit;
Figure 60 shows the coded port protocol;
Figure 61 shows the start code detector;
Figure 62 shows start codes detected and converted to Tokens;
Figure 63 shows the start codes detector passing Tokens;
Figure 64 shows overlapping MPEG start codes (byte aligned);
Figure 65 shows overlapping MPEG...Figure 79 shows an overview of MPEG inverse quantization;
Figure 80 shows a quantization table memory map;
Figure 81 shows an overview of JPEG baseline sequential structure;
Figure 82 shows a tokenised JPEG picture;
Figure 83 shows a temporal decoder;
Figure 84 shows a picture buffer specification;
Figure 85 shows an...pipeline, such conditioning including reconfiguring of the processing stages. Still other tokens may provide both data and conditioning to the processing stages in the pipeline. Some of said tokens may identify coding standards to the processing stages in the pipeline, whereas other tokens may operate independent of any coding standard among...

...encoded bit streams arranged as a serial bit stream of digital bits and having separately encoded pairs of start codes and data carried in the **serial** bit stream, a Start Code Detector subsystem having first, second and third registers connected in **serial** fashion, each of the registers storing a different number of bits from the bit stream, the first register storing a value, the second register and...of pipeline stages. Furthermore, data may be processed in more than one stage and the processing time for different stages can differ.

In addition to **clock** and data signals (described below), the pipeline includes two transfer control signals -- a "VALID" signal and an "ACCEPT" signal. These signals are used to control...3) illustrate generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping **clock** with phases (o slash)0 and (o slash)1. Although a two-phase **clock** is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a **clock** with more than two phases.

As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and...

...the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is snown in Fig. 3. A change of state during a **clock** phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a ...

...HIGH whenever the storage elements contain valid data.

In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping **clock** phases (o slash)0 and (o slash)1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during **clock** cycle (o slash)1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the **clock** cycle (o slash)0. Fig. 3 also illustrates that the primary and secondary storage elements in each stage are further connected via an internal acceptance...ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective **clock** phases until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the ol...

...storage elements (within the same stage or within the preceding pipeline stage). Rather, this change propagates upstream within the pipeline one storage element block per **clock** phase.

As this example illustrates, the concept of a "stage" in the pipeline structure illustrated in Fig. 3 is to some extent a matter of...signal LOW not only when all of the downstream storage elements are filled with valid data, but also when a stage requires more than one **clock** phase to finish processing its data. This also can occur when it creates valid data in one or both of its storage elements. In other...

...process analog signals.

As discussed previously, while other conventional timing arrangements may be used, the interface is preferably controlled by a two-phase, non-overlapping **clock**. In Figs. 4-9, these **clock** phase signals are referred to as PH0 and PH1. In Fig. 4, a line is shown for each **clock** phase signal.

Input data enters a pipeline stage over a multi-bit data bus IN(underscore)DATA and is transferred to a **following** pipeline stage

or to subsequent receiving circuitry over an output data bus OUT(underscore)DATA. The input data is first loaded in a manner described ...

...example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs, that is, they are "loaded", when the clock input is HIGH, i.e., at a logic "1" level. Additionally, the Q outputs hold their last values. In other words, the Q outputs are "latched" on the falling edge of their respective clock signals. Each latch has for its clock either one of two non-overlapping clock signals PH0 or PH1 (as shown in Fig. 5), or the logical AND combination of one of these clock signals PH0, PH1 and one logic signal. The invention works equally well, however, by providing latches that latch on the rising edges of the clock signals, or any other known latching arrangement, as long as conventional methods are applied to ensure proper timing of the latching operations.

The output data...the Q signal and/or its logical inverse.

The data and validation latches LDIN, LDOUT, LVIN and LVOUT, load their respective data inputs when both clock signals (PH0 at the input side and PH1 at the output side) and the output from the acceptance latch of the same side are logical "1". Thus, the clock signal (PH0 for the input latches LDIN and LVIN) and the output of the respective acceptance latch (in this case, LAIN) are used in a...

...and QAIN are both "1". It will latch this data when either of these two signals goes to a "0".

Although only one of the clock phase signals PH0 or PH1, is used to clock the data and validation latches at the input (and output) side of the pipeline stage, the other clock phase signal is used, directly, to clock the acceptance latch at the same side. In other words, the acceptance latch on either side (input or output) of a pipeline stage is preferably clocked "out of phase" with the data and validation latches on the same side. For example, PH1 is used to clock the acceptance input latch, although PH0 is used in generating the clock signal CK for the data latch LDIN and the validation latch LVIN.

As an example of the operation of a pipeline augmented by the two... signal IN(underscore)VALID to the illustrated stage has not gone to a "1" since the system was most recently reset. Assume further that several clock cycles have taken place since the system was last reset and, accordingly, the circuitry has reached a steady-state condition. The validation input signal QVIN from the validation latch LVIN is, therefore, loaded as a "0" during the next positive period of the clock PH0. The input to the acceptance input latch LAIN (via the gate NAND1 or another equivalent gate), is, therefore, loaded as a "1" during the next positive period of the clock signal PH1. In other words, since the data in the data input latch LDIN is not valid, the stage signals that it is ready to...

...transparent latches so that whatever data is on the IN(underscore)DATA bus simply is loaded into the data latch LDIN as soon as the clock signal PH0 goes to a "1". Of course, this invalid data will also be loaded into the next data latch LDOUT of the following pipeline...

...a data latch does not contain valid data, it accepts or "loads" any data presented to it during the next positive period of its respective clock signal. On the other hand, such invalid data is not loaded in any stage for which the acceptance signal from its corresponding acceptance latch is...

...by rising to a "1". The output of the corresponding validation latch

then rises to a "1" on the next rising edge of its respective clock phase signal. For example, the validation input signal QVIN of latch LVIN rises to a "1" when its corresponding IN(underscore)VALID signal goes high (that is, rises to a "1") on the next rising edge of the clock phase signal PH0.

Assume now, instead, that the data input latch LDIN contains valid data. If the data output latch LDOUT is ready to accept new data, its acceptance signal QAOUT will be a "1". In this case, during the next positive period of the clock signal PH1, the data latch LDOUT and validation latch LVOUT will be enabled, and the data latch LDOUT will load the data present at its input. This will occur before the next rising edge of the other clock signal PH0, since the clock signals are non-overlapping. At the next rising edge of PH0, the preceding data latch (LDIN) will, therefore, not latch in new input data from...

...latches (within a stage or between adjacent stages) that are able to accept data, since they will be operating based on alternate phases of the clock. Any data latch that is not ready to accept new data because it contains valid data that cannot yet be passed, will have an output...

...or reset state whenever a valid transmission begins and the reset signal goes HIGH. The reset signal NOTRESET0, therefore, operates as a digital "ON/OFF" switch, such that it must be at a HIGH value in order to activate the pipeline.

Note that it is not necessary to reset all of...

...the state of the validation input signal QVIN. The acceptance input signal QAIN then rises to a "1" at the next rising edge of the clock signal PH1. Assuming that the validation signal IN(underscore)VALID has been correctly reset to a "0", then upon the subsequent rising edge of the clock signal PH0, the output from the validation latch LVIN will become a "0", as it would have done if it had been reset directly.

As...

...latch: If the reset signal NOTRESETO can be guaranteed to be low during more than one complete cycle of both phases PH0, PH1 of the clock, then the "automatic reset" (a backwards propagation of the reset signal) will occur for validation latches in preceding pipeline stages. Indeed, if the reset signal is held low for at least as many full cycles of both phases of the clock as there are pipeline stages, it will only be necessary to directly reset the validation output latch in the final pipeline stage.

Figs. 5a and 5b (referred to collectively as Fig. 5) illustrate a timing diagram showing the relationship between the non-overlapping clock signals PH0, PH1, the effect of the reset signal, and the holding and transfer of data for the different permutations of validation and acceptance signals...the stage depends upon stored state information, which is another way of saying it must retain some information about its own history one or more clock cycles ago. The present invention is well-suited for use in pipelines that include such "state machine" stages, as well as for use in applications...

...The value of the extension bit is loaded into LEIN and is then loaded into LEOUT on the next rising edge of the non-overlapping clock phase signal PH1. Latch LEOUT, thus, contains the value of the current extension bit, but only during the second half of the non-overlapping, two-phase clock. Latch LEPREV, however, loads this extension bit value on the next rising edge of the clock signal PHO, that is, the

same signal that enables the extension bit input latch LEIN. The output QEPREV of the latch LEPREV, thus, will hold the value of the extension bit during the previous PHO clock phase.

The five bits of the data word output from the inverting Q output, plus the non-inverted MD(2), of the latch LDIN are...signals and the inverting output of the validation latches LVIN and LVOUT, respectively. This illustrates one way in which the gates NAND1/2 and INV1/2 in Fig. 4 can be replaced if the latches have inverting outputs.

Although this is an extremely simple example of a "state-dependent" pipeline stage, i.e., since it depends on...

...of the extension bit at the input and at the output of the stage, respectively. As Fig. 8a shows, the input extension latch LEIN is clocked synchronously with the input data latch LDIN and the validation signal IN(underscore)VALID.

For ease of reference, the various latches included in the duplication ...of the intermediate extension bit (labeled "MID(underscore)EXTN" and as signal S4), and it loads this value on the next rising edge of the clock phase PHO into the latch LI1, whose output is the bit QI1 and is one of the inputs to the token decoding logic group that...

...both QI1 and S1 are HIGH, the signal DATA(underscore)TOKEN will retain its state (whether "0" or "1"). This is true even though the clock signals PHO and PH1 are clocking the latches (LI2 and LO2 respectively). The value of DATA(underscore)TOKEN can only change when one or both of the signals QI1 and S1...

...S2 will thus be a "0". As a result, this "0" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "0", indicating that the circuitry is not processing a DATA token.

If QI1 is "0" and...

...NAND22 from the output of NAND20). As a result, this "1" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "1", indicating that the circuitry is processing a DATA token.

The NOT(underscore)DUPLICATE signal (the output signal QO3) is similarly loaded into the latch LI3 on the next rising edge of the clock PHO. The output signal QI3 from the latch LI3 is combined with the output signal QI2 in a gate NAND24 to form the signal S3...

...is not a duplicate (QI3 = 0), then the signal S3 goes high.

Assume now, that the DATA TOKEN signal remains HIGH for more than one clock signal. Since the NOT(underscore)DUPLICATE signal (QO3) is "fed back" to the latch LI3 and will be inverted by the gate NAND 24 (since...states, so that the input latches will be enabled and will be able to accept data, at most, during every other complete cycle of both clock phases PH0, PH1. The additional condition that the following stage be prepared to accept data, as indicated by a "HIGH" OUT(underscore)ACCEPT signal, must...

...be satisfied. The output latch LDOUT will, therefore, place the same data word onto the output bus OUT(underscore)DATA for at least two full clock cycles. The OUT(underscore)VALID signal will be a "1" only when there is both a valid DATA(underscore)TOKEN (QO2 HIGH) and the validation...

...is a duplicate (QI3 is a "O"). If the signal MID(underscore)ACCEPT is HIGH, the latches LO1-LO3 will, therefore, be enabled when the clock signal PH1 is high whenever valid input data is loaded at the input of the stage, or when the latched data is a duplicate.

From...on the downstream latch LVOUT, with the reset signal being propagated backwards to cause the upstream validation latch to be forced low on the next clock cycle.

It should be noted that in the example shown in Fig. 8, the duplication of data contained in DATA tokens serves only as an example...

...timing diagram for the data duplication circuit shown in Figs. 8a and 8b. As before, the timing diagram shows the relationship between the two-phase clock signals, the various internal and external control signals, and the manner in which data is clocked between the input and output sides of the stage and is duplicated.

Referring now more particularly to Figure 10, there is shown a reconfigurable process...In a first embodiment, in accordance with the present invention, as previously described with reference to Figures 10-12 an address generator is employed to store a block of formatted data, output from either the first decoder (Spatial Decoder) or the combination of the first decoder (Spatial Decoder) and the second... H.261 compression standard. The MPU in such prior machines generates signals stating in multiple different places within the machine that the compression standard is changing. The MPU makes changes at different times and, in addition, may flush the pipeline through.

In accordance with the invention, by issuing a change of CODING(underscore)STANDARD tokens at the...world, e.g. PAL-NTSC television standards. This is accomplished by selectively dropping or repeating pictures in a manner which is unique. Ordinary "frame rate converters," e.g. 2-3 pulldown, operate with a fixed input picture rate, whereas the Video Formatter can handle a variable input picture rate.

6. RECONFIGURABLE PROCESSING STAGE

Referring...

...RPS, it is decoded in the token decode circuit 33 and appropriate action will be taken. If it is not recognized, it will be passed unchanged to the output two-wire interface 42 through the output circuit 41. The present invention operates as a pipeline processor having a two-wire interface...tokens are generated by circuitry within the decoder processor and emulate the operation of a number of different type standard-dependent signals passing into the serial pipeline processor for handling. The technique used is to study all the parameters of the multi-standards that are selected for processing by the serial processor and noting 1) their similarities, 2) their dissimilarities, 3) their needs and requirements and 4) selecting the correct token function to effectively process all...needs to provide the most information to the processing unit so that it can start the decompression with as much information as possible. Words which follow later are typically shorter in length because they contain the difference signals comparing the first word with reference to the second position on the scan information field.

The words are interspersed with each other, as required by the standard encoding system, so that variable amounts of...

...construction of both the address generator and the DRAM interface, as discussed further below.

In the present invention, the DRAM interface can operate from a clock which is asynchronous to both the address generator and to the clocks of the stages through which data is passed. Special techniques have been used to handle this asynchronous nature of the operation.

Data is typically transferred...an address, it waits for the address generator to supply a valid address, processes that address and then sets

the accept line high for one clock period. Thus, it implements a request/acknowledge (REQ/ACK) protocol.

A unique feature of the DRAM interface 302 is its ability to communicate independently with...

...control and sends a signal to the read side to indicate that RAM1 is now ready to be read. This signal passes between two asynchronous clock regimes and, therefore, passes through three synchronizing flip flops.

Provided RAM2 312 is empty, the next item of data to arrive on the input side...DRAM interface that less than 64 bytes should be read (this may be required at the beginning or end of a raster line), although a multiple of 8 bytes is always read. This is achieved by using start and stop values. The start value is used for the top part of...

...block in the present invention uses timing chains to place the edges of the DRAM signals to a precision of a quarter of the system clock period. Two quadrature clocks from the phase locked loop are used. These are combined to form a notional 2x clock. Any one chain is then made from two shift registers in parallel, on opposite phases of the 2x clock.

First of all, there is one chain for the page start cycle and another for the read/write/refresh cycles. The length of each cycle...

...is created. The pulse travels along the chains and is directed by the state information from the DRAM interface. The pulse generates the DRAM interface clock. Each DRAM interface clock period corresponds to one cycle of the DRAM, consequently, as the DRAM cycles have different lengths, the DRAM interface clock is not at a constant rate.

Moreover, additional timing chains combine the pulse from the above chains with the information from the DRAM interface to...interface (MPI) is used on all circuits with in the Spatial Decoder and Temporal Decoder. The MPI operates asynchronously with various Spatial and Temporal Decoder clocks. Referring to Table A.6.1 of the subsequent further detailed description, there is shown the various MPI signals that are used on this interface...is set forth in the following sections.

. Description of features common to chips in the chip-set:
. Tokens
. Two wire interfaces
. DRAM interface
. Microprocessor interface
. Clocks
. Description of the Spatial Decoder chip
. Description of the Temporal Decoder chip

SECTION A.1

The first description section covers the majority of the electrical...

...2:0

. Flexible chroma sampling formats
. Full JPEG baseline decoding
. Glue-less page mode DRAM interface
. 208 pin PQFP package
. Independent coded data and decoder clocks
. Re-orders MPEG picture sequence

The Video decoder family provides a low chip count solution for implementing high resolution digital video decoders. The chip-set...to control the flow of information. Data is only transferred between blocks when both the sender and receiver are observed to be ready when the clock rises.

1)Data transfer
2)Receiver not ready

3)Sender not ready
If the sender is not ready (as in 3 Sender not ready above...

...PCB tracks between chips. Where possible, track lengths should be kept below 25 mm. The PCB track capacitance should be kept to a minimum.
The clock distribution should be designed to minimize the clock slew between chips. If there is any clock slew, it should be arranged so that "receiving chips" see the clock before "sending chips".1) Note: Figure 38 shows the two-wire interface between the system de-mux chip and the coded data port of the Spatial Decoder operating from the main decoder clock. This is optional as this two wire interface can work from the coded data clock which can be asynchronous to the decoder clock. See Section A.10.5, "Coded data clock". Similarly the display interface of the Image Formatter can operate from a clock that is asynchronous to the main decoder clock.)
1))

All chips communicating via two wire interfaces should operate from the same digital power supply.

A.4.5 Interface timing

A.4.6 - Signal...

...Table A.4.3 are those for V1H)) and V1L)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V.

A.4.7 Control clock
In general, the clock controlling the transfers across the two wire interface is the chip's decoder(underscore)clock. The exception is the coded data port input to the Spatial Decoder. This is controlled by coded(underscore)clock. The clock signals are further described herein.

SECTION A.5 DRAM Interface

A.5.1 The DRAM interface
A single high performance, configurable, DRAM interface is used... registers of the present invention can be read at any time.

A.5.4 Interface timing (ticks)
The DRAM interface timing is derived from a Clock which is running at four times the input Clock rate of the device (decoder(underscore)clock). This clock is generated by an on-chip PLL.
For brevity, periods of this high speed clock are referred to as ticks.

A.5.5 Interface registers

A.5.6 Interface operation
The DRAM interface uses fast page mode. Three different types... determined by the register, refresh(underscore)interval.
The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 decoder(underscore)clock cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface to continuously...

...ordinary skill in the art will appreciate that microprocessor interfaces of other widths may also be used. The MPI operates synchronously to various decoder chip **clocks**.

A.6.1 MPI signals

A.6.2 - MPI electrical specifications

A.6.2.1 AC characteristics

A.6.3 Interrupts
In accordance with the...have no application in the normal use of the devices and need not be accessed by normal device configuration and control software.

SECTION A.7 **Clocks**
In accordance with the present inventions, many different **clocks** can be identified in the video decoder system. Examples of **clocks** are illustrated in Figure 56.
As data passes between different **clock** regimes within the video decoder chip-set, it is resynchronized (on-chip) to each new **clock**. In the present invention, the maximum frequency of any input **clock** is 30 MHz)). However, one of ordinary skill in the art will appreciate that other frequencies, including those greater than 30MHz, may also be used. On each chip, the microprocessor interface (MPI) operates asynchronously to the chip **clocks**. In addition, the Image Formatter can generate a low frequency audio **clock** which is synchronous to the decoded video's picture rate. Accordingly, this **clock** can be used to provide audio/video synchronization.

A.7.1 Spatial Decoder **clock** signals
The Spatial Decoder has two different (and potentially asynchronous) **clock** inputs:

A.7.2 Temporal Decoder **clock** signals
The Temporal Decoder has only one **clock** input:

A.7.3 Electrical specifications

A.7.3.1 CMOS levels
The **clock** input signals are CMOS inputs. VIHmin)) is approx. 70% of VDD)) and VILmax)) is approx. 30% of VDD)). The values shown in Table A.7.4 are those for VIH)) and VIL)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V.
A.7.3.2 Stability of **clocks**
In the present invention, **clocks** used to drive the DRAM interface and the chip-to-chip interfaces are derived from the input **clock** signals. The timing specifications for these interfaces assume that the input **clock** timing is stable to within (+-) 100 ps.

SECTION A.8 JTAG
As circuit boards become more densely populated, it is increasingly difficult to verify the...

...pins. The trst (Test Reset) pin resets the JTAG circuitry, to ensure that the device doesn't power-up in test mode. The tck (Test **Clock**) pin is used to **clock** serial test patterns into the tdi (Test Data

Input) pin, and out of the tdo (Test Data Output) pin. Lastly, the operational mode of the JTAG circuitry is set by clocking the appropriate sequence of bits into the tms (Test Mode Select) pin.

The JTAG standard is extensible to provide for additional features at the discretion...

...Full JPEG baseline decoding
. Glue-less DRAM interface
. Single +5V supply
. 208 pin PQFP package
. Max. power dissipation 2.5W
. Independent coded data and decoder clocks
. Uses standard page mode DRAM

The Spatial Decoder is a configurable VLSI decoder chip for use in a variety of JPEG, MPEG and H.261...sampled at the same time as data (7:0), coded(underscore)extn and coded(underscore)valid, i.e., on the rising edge of coded(underscore)clock.

A.10.1.2 Byte mode

If, however, byte(underscore)mode is high, then a byte of data is transferred on data(7:0) under...

...Token header to be generated on-chip. Any further bytes transferred in byte mode are thereafter appended to this DATA Token until the input mode changes. Recall, DATA Tokens can contain as many bits as are necessary.

The MPI register bit, coded busy, and the signal, coded(underscore)accept, indicate on...

...A.11). The Start code Detector analyses data in the DATA Tokens bit serially. The Detector's normal rate of processing is one bit per clock cycle (of coded(underscore)clock). Accordingly, it will typically decode a byte of coded data every 8 cycles of coded(underscore) clock. However, extra processing cycles are occasionally required, e.g., when a non-DATA Token is supplied or when a start code is encountered in the...

...buffer newly arriving coded data (or stop new data for arriving) if the Spatial decoder is unable to accept data.

A.10.5 Coded data clock

In accordance with the present invention, the coded data port, the input circuit and other functions in the Spatial Decoder are controlled by coded(underscore)clock. Furthermore, this clock can be asynchronous to the main decoder(underscore)clock. Data transfer is synchronized to decoder(underscore)clock on-chip.

SECTION A.11 Start code detector

A.11.1 Start codes

As is well known in the art, MPEG and H.261 coded...

...the start-up of the decoder.

A.11.2 Start code detector registers

As previously discussed, many of the Start Code Detector registers are in constant use by the Start Code Detector. So, accessing these registers will be unreliable if the Start Code Detector is processing data. The user is responsible...of the buffers ensures that the buffers never empty during decoding and, this, therefore ensures that the decoder is able to decode new pictures at regular intervals.

Generally, two facilities are required to correctly start-up a decoder. First, there must be a mechanism to measure how much data has been provided...

...up delay for the first picture, the requirements of all subsequent pictures will be met automatically.

MPEG, therefore, specifies the start-up requirements as a **delay**. However, in a **constant** bit rate system this **delay** can readily be converted to a bit count. This is the basis on which the start-up control of the Spatial Decoder of the present...four main processing blocks in the Video Demux: Parser State Machine, Huffman decoder (including an ITOD), Macroblock counter and ALU.

The Parser or state machine **follows** the syntax of the coded video data and instructs the **other** units. The Huffman decoder **converts** variable length coded (VLC) data into integers. The Macroblock counter keeps track of which section of a picture is being decoded. The ALU performs the...

37/3,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

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Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
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CLAIMS A (English) 199902 662
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SPEC A (English) 199902 126651
SPEC B (English) 200119 120956
Total word count - document A 127332
Total word count - document B 123385
Total word count - documents A + B 250717

...ABSTRACT universal adaptation units for interfacing with said stages and interacting with selected stages, said two-wire interfaces each comprising:
a sender,
a receiver , and
a **clock** connected to said sender and said receiver, said **clock** having transitions from
a first state to a second state,

wherein data is transferred from said sender to said receiver upon a **clock** transition only when said sender is ready and said receiver is ready;

said processing stages comprising an image formatter receiving said tokens via a first...

...SPECIFICATION of the number of components, for a linear-phase filter, and zero-padded to equal the number of samples of a data block, this being **followed** by forming the discrete odd cosine **transform** (DOCT) of the padded kernel matrix.
United States Patent No. 5,175,617 discloses a system and method for transmitting logmap video images through telephone...

...the proposed ISO/IEC MPEG standards. Included are three cooperating components or subsystems that operate to variously adaptively pre-process the incoming digital motion video **sequences**, allocate bits to the pictures in a **sequence**, and adaptively quantize **transform** coefficients in **different** regions of a picture in a video **sequence** so as to provide optimal visual quality given the number of bits allocated to that picture.
United States Patent No. 5,267,334 discloses a method of removing frame redundancy in a computer system for a **sequence** of moving images. The method comprises detecting a first scene **change** in the **sequence** of moving images and generating a first keyframe containing complete scene information for a first image. The first keyframe is known, in a preferred embodiment...
...following the first image in time in the sequence of moving images. This at least one frame being known as an interframe. Finally, detecting a **second** scene **change** in the **sequence** of moving images and generating a second keyframe containing complete scene information for an image displayed at the ...block signal in most cases.
United States Patent No. 4,903,018 discloses a process and data processing system for compressing and expanding structurally associated **multiple** data **sequences**. The process is particular to data sets in which an analysis is made of the structure in order to identify a characteristic common to a...present invention may also include tokens in the form of a PICTURE(underscore)START code token for indicating that the start of a picture will **follow** in the subsequent DATA token, a PICTURE(underscore)END token for indicating the end of an individual picture, a FLUSH token for clearing buffers and...

...an inverse modeller means active upon the data stream from a token for expanding out the run level code to a run of zero data **followed** by a level, whereby each token is expressed with a specified number of values. The invention also includes an inverse modeller stage, an inverse discrete...2) illustrate the control of data transfer between stages of a preferred embodiment of a pipeline using a two-wire interface and a multi-phase **clock**;

Figure 4 is a block diagram that illustrates a basic embodiment of a pipeline stage that incorporates a two-wire transfer control and also shows...

...in an exemplifying "data duplication" pipeline stage;

Figures. 9a and 9b taken together depict one example of a timing diagram that shows the two-phase **clock**, the two-wire transfer control signals and the other internal data and control signals used in the exemplifying embodiment Shown in Figures. 8a and 8b...

...shows a macroblock structure;

Figure 37 shows a two-wire interface protocol;
Figure 38 shows the location of external two-wire interfaces;
Figure 39 shows **clock** propagation;
Figure 40 shows two-wire interface timing;
Figure 41 shows examples of access structure;
Figure 42 shows a read transfer cycle;
Figure 43 shows...

...timing;

Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory map;
Figure 56 shows a typical decoder **clock** regime;
Figure 57 shows input **clock** requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit;
Figure 60 shows the coded port protocol...encoded bit streams arranged as a serial bit stream of digital bits and having separately encoded pairs of start codes and data carried in the **serial** bit stream, a Start Code Detector subsystem having first, **second** and third registers connected in **serial** fashion, each of the registers storing a different number of bits from the bit stream, the first register storing a value, the second register and...of pipeline stages. Furthermore, data may be processed in more than one stage and the processing time for different stages can differ.

In addition to **clock** and data signals (described below), the pipeline includes two transfer control signals -- a "VALID" signal and an "ACCEPT" signal. These signals are used to control...3) illustrate generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping **clock** with phases (o slash)0 and (o slash)1. Although a two-phase **clock** is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a **clock** with more than two phases.

As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and...

...the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is snown in Fig. 3. A change of state during a **clock** phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a ...

...HIGH whenever the storage elements contain valid data.

In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping clock phases (o slash)0 and (o slash)1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during clock cycle (o slash)1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the clock cycle (o slash)0. Fig. 3 also illustrates that the primary and secondary storage elements in each stage are further connected via an internal acceptance...ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective clock phases until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the ol...

...storage elements (within the same stage or within the preceding pipeline stage). Rather, this change propagates upstream within the pipeline one storage element block per clock phase.

As this example illustrates, the concept of a "stage" in the pipeline structure illustrated in Fig. 3 is to some extent a matter of... ACCEPTsignal LOW not only when all of the downstream storage elements are filled with valid data, but also when a stage requires more than one clock phase to finish processing its data. This also can occur when it creates valid data in one or both of its storage elements. In other...

...process analog signals.

As discussed previously, while other conventional timing arrangements may be used, the interface is preferably controlled by a two-phase, non-overlapping clock. In Figs. 4-9, these clock phase signals are referred to as PH0 and PH1. In Fig. 4, a line is shown for each clock phase signal.

Input data enters a pipeline stage over a multi-bit data bus IN(underscore)DATA and is transferred to a following pipeline stage... ...which constitute the secondary storage elements described above.

In the illustrated example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs, that is, they are "loaded", when the clock input is HIGH, i.e., at a logic "1" level. Additionally, the Q outputs hold their last values. In other words, the Q outputs are "latched" on the falling edge of their respective clock signals. Each latch has for its clock either one of two non-overlapping clock signals PH0 or PH1 (as shown in Fig. 5), or the logical AND combination of one of these clock signals PH0, PH1 and one logic signal. The invention works equally well, however, by providing latches that latch on the rising edges of the clock signals, or any other known latching arrangement, as long as conventional methods are applied to ensure proper timing of the latching operations.

The output data...the Q signal and/or its logical inverse.

The data and validation latches LDIN, LDOUT, LVIN and LVOUT, load their respective data inputs when both clock signals (PH0 at the input side and PH1 at the output side) and the output from the acceptance latch of the same side are logical "1". Thus, the clock signal (PH0 for the input latches LDIN and LVIN) and the output of the respective acceptance latch (in this case, LAIN) are used in a...

...and QAIN are both "1". It will latch this data when either of these two signals goes to a "0".

Although only one of the clock phase signals PH0 or PH1, is used to clock the data and validation latches at the input (and output) side of the pipeline stage, the other clock phase signal is used, directly, to clock the acceptance latch at the same side. In other

words, the acceptance latch on either side (input or output) of a pipeline stage is preferably clocked "out of phase" with the data and validation latches on the same side. For example, PH1 is used to clock the acceptance input latch, although PH0 is used in generating the clock signal CK for the data latch LDIN and the validation latch LVIN.

As an example of the operation of a pipeline augmented by the two... signal IN(underscore)VALID to the illustrated stage has not gone to a "1" since the system was most recently reset. Assume further that several clock cycles have taken place since the system was last reset and, accordingly, the circuitry has reached a steady-state condition. The validation input signal QVIN from the validation latch LVIN is, therefore, loaded as a "0" during the next positive period of the clock PH0. The input to the acceptance input latch LAIN (via the gate NAND1 or another equivalent gate), is, therefore, loaded as a "1" during the next positive period of the clock signal PH1. In other words, since the data in the data input latch LDIN is not valid, the stage signals that it is ready to...

...transparent latches so that whatever data is on the IN(underscore)DATA bus simply is loaded into the data latch LDIN as soon as the clock signal PH0 goes to a "1". Of course, this invalid data will also be loaded into the next data latch LDOUT of the following pipeline...

...a data latch does not contain valid data, it accepts or "loads" any data presented to it during the next positive period of its respective clock signal. On the other hand, such invalid data is not loaded in any stage for which the acceptance signal from its corresponding acceptance latch is...

...by rising to a "1". The output of the corresponding validation latch then rises to a "1" on the next rising edge of its respective clock phase signal. For example, the validation input signal QVIN of latch LVIN rises to a "1" when its corresponding IN(underscore)VALID signal goes high (that is, rises to a "1") on the next rising edge of the clock phase signal PH0.

Assume now, instead, that the data input latch LDIN contains valid data, If the data output latch LDOUT is ready to accept new data, its acceptance signal QAOUT will be a "1". In this case, during the next positive period of the clock signal PH1, the data latch LDOUT and validation latch LVOUT will be enabled, and the data latch LDOUT will load the data present at its input, This will occur before the next rising edge of the other clock signal PH0, since the clock signals are non-overlapping. At the next rising edge of PH0, the preceding data latch (LDIN) will, therefore, not latch in new input data from...

...latches (within a stage or between adjacent stages) that are able to accept data, since they will be operating based on alternate phases of the clock. Any data latch that is not ready to accept new data because it contains valid data that cannot yet be passed, will have an output...

...the state of the validation input signal QVIN. The acceptance input signal QAIN then rises to a "1" at the next rising edge of the clock signal PH1. Assuming that the validation signal IN(underscore)VALID has been correctly reset to a " ...latch: If the reset signal NOTRESETO can be guaranteed to be low during more than one complete cycle of both phases PH0. PH1 of the clock, then the "automatic reset" (a backwards propagation of the reset signal) will occur for validation latches in preceding pipeline stages. Indeed, if the

reset signal is held low for at least as many full cycles of both phases of the clock as there are pipeline stages, it will only be necessary to directly reset the validation output latch in the final pipeline stage.

Figs. 5a and 5b (referred to collectively as Fig. 5) illustrate a timing diagram showing the relationship between the non-overlapping clock signals PH0, PH1, the effect of the reset signal, and the holding and transfer of data for the different permutations of validation and acceptance signals...thus, depends on its previous states. In other words, the stage depends upon stored state information, which is another way of saying it must retain some information about its own history one or more clock cycles ago. The present invention is well-suited for use in pipelines that include such "state machine" stages, as well as for use in applications...

...The value of the extension bit is loaded into LEIN and is then loaded into LEOUT on the next rising edge of the non-overlapping clock phase signal PH1. Latch LEOUT, thus, contains the value of the current extension bit, but only during the second half of the non-overlapping, two-phase clock. Latch LEPREV, however, loads this extension bit value on the next rising edge of the clock signal PHO, that is, the same signal that enables the extension bit input latch LEIN. The output QEPREV of the latch LEPREV, thus, will hold the value of the extension bit during the previous PHO clock phase.

The five bits of the data word output from the inverting Q output, plus the non-inverted MD(2), of the latch LDIN are...of the extension bit at the input and at the output of the stage, respectively. As Fig. 8a shows, the input extension latch LEIN is clocked synchronously with the input data latch LDIN and the validation signal IN(underscore)VALID.

For ease of reference, the various latches included in the duplication ...of the intermediate extension bit (labeled "MID(underscore)EXTN" and as signal S4), and it loads this value on the next rising edge of the clock phase PHO into the latch LI1, whose output is the bit QI1 and is one of the inputs to the token decoding logic group that...

...both QI1 and S1 are HIGH, the signal DATA(underscore)TOKEN will retain its state (whether "0" or "1"). This is true even though the clock signals PHO and PH1 are clocking the latches (L12 and LO2 respectively). The value of DATA(underscore)TOKEN can only change when one or both of the signals QI1 and S1...

...S2 will thus be a "0". As a result, this "0" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "0", indicating that the circuitry is not processing a DATA token.

If QI1 is "0" and...

...NAND22 from the output of NAND20). As a result, this "1" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "1", indicating that the circuitry is processing a DATA token.

The NOT(underscore)DUPLICATE signal (the output signal QO3) is similarly loaded into the latch LI3 on the next rising edge of the clock PHO. The output signal QI3 from the latch LI3 is combined with the output signal QI2 in a gate NAND24 to form the signal S3...

...is not a duplicate (QI3= 0), then the signal S3 goes high.

Assume now, that the DATA TOKEN signal remains HIGH for more than one clock signal. Since the NOT(underscore)DUPLICATE signal (QO3) is "fed back" to the latch LI3 and will be inverted by the gate NAND 24 (since...states, so that the input latches will be enabled and will be

able to accept data, at most, during every other complete cycle of both clock phases PH0, PH1. The additional condition that the following stage be prepared to accept data, as indicated by a "HIGH" OUT(underscore)ACCEPT signal, must...

...course, still be satisfied. The output latch LDOUT will, therefore, place the same data word onto the output bus OUT(underscore)DATA for at least two full clock cycles. The OUT(underscore)VALID signal will be a "1" only when there is both a valid DATA(underscore)TOKEN (QO2 HIGH) and the validation...

...is a duplicate (QI3 is a "O"). If the signal MID(underscore)ACCEPT is HIGH, the latches LO1-LO3 will, therefore, be enabled when the clock signal PH1 is high whenever valid input data is loaded at the input of the stage, or when the latched data is a duplicate.

From...on the downstream latch LVOUT, with the reset signal being propagated backwards to cause the upstream validation latch to be forced low on the next clock cycle.

It should be noted that in the example shown in Fig. 8, the duplication of data contained in DATA tokens serves only as an...

...a timing diagram for the data duplication circuit shown in Figs. 8aand 8b. As before, the timing diagram shows the relationship between the two-phase clock signals, the various internal and external control signals, and the manner in which data is clocked between the input and output sides of the stage and is duplicated.

Referring now more particularly to Figure 10, there is shown a reconfigurable process...additional detailed description of illustrative embodiment of the invention which, for purposes of clarity and convenience of explanation are grouped and set forth in the following sections:

1. Multi-Standard Configurations
2. JPEG Still Picture Decoding
3. Motion Picture Decompression
4. RAM Memory Map
5. Bitstream Characteristics
6. Reconfigurable Processing Stage...

...In a first embodiment, in accordance with the present invention, as previously described with reference to Figures 10-12 an address generator is employed to store a block of formatted data, output from either the first decoder (Spatial Decoder) or the combination of the first decoder (Spatial Decoder) and the second...world, e.g. PAL-NTSC television standards. This is accomplished by selectively dropping or repeating pictures in a manner which is unique. Ordinary "frame rate converters," e.g. 2-3 pulldown, operate with a fixed input picture rate, whereas the Video Formatter can handle a variable input picture rate.

6. RECONFIGURABLE PROCESSING STAGE

Referring...tokens are generated by circuitry within the decoder processor and emulate the operation of a number of different type standard-dependent signals passing into the serial pipeline processor for handling. The technique used is to study all the parameters of the multi-standards that are selected for processing by the serial processor and noting 1) their similarities. 2) their dissimilarities, 3) their needs and requirements and 4) selecting the correct token function to effectively process all of the standard signals sent into the...construction of both the address generator and the DRAM interface, as discussed further below.

In the present invention, the DRAM interface can operate from a clock which is asynchronous to both the address generator and to the clocks of the stages through which data is passed. Special

techniques have been used to handle this asynchronous nature of the operation.

Data is typically transferred...an address, it waits for the address generator to supply a valid address, processes that address and then sets the accept line high for one clock period. Thus, it implements a request/acknowledge (REQ/ACK) protocol.

A unique feature of the DRAM interface 302 is its ability to communicate independently with...

...control and sends a signal to the read side to indicate that RAM1 is now ready to be read. This signal passes between two asynchronous clock regimes and, therefore, passes through three synchronizing flip flops.

Provided RAM2 312 is empty, the next item of data to arrive on the input side...

...in the same DRAM page. In this way, full use can be made of DRAM fast page access modes, where one row address is supplied followed by many column addresses. In particular, row addresses are supplied by the address generator, while column addresses are supplied by the DRAM interface, as discussed...The Temporal Decoder's addressing is more complex because of its predictive aspects as discussed further in this section. The video formatter's addressing is more complex because of multiple video output standard aspects, as discussed further in the sections relating to the video formatter.

As mentioned previously, the Temporal Decoder...block in the present invention uses timing chains to place the edges of the DRAM signals to a precision of a quarter of the system clock period. Two quadrature clocks from the phase locked loop are used. These are combined to form a notional 2x clock. Any one chain is then made from two shift registers in parallel, on opposite phases of the 2x clock.

First of all, there is one chain for the page start cycle and another for the read/write/refresh cycles. The length of each cycle...

...is created. The pulse travels along the chains and is directed by the state information from the DRAM interface. The pulse generates the DRAM interface clock. Each DRAM interface clock period corresponds to one cycle of the DRAM, consequently, as the DRAM cycles have different lengths, the DRAM interface clock is not at a constant rate.

Moreover, additional timing chains combine the pulse from the above chains with the information from the DRAM interface to...interface (MPI) is used on all circuits with in the Spatial Decoder and Temporal Decoder. The MPI operates asynchronously with various Spatial and Temporal Decoder clocks. Referring to Table A.6.1 of the subsequent further detailed description, there is shown the various MPI signals that are used on this interface...tokens, as discussed further in the token section. Note that most of the data will be DATA tokens that require decoding.

The in shifter 323 serially passes data to the Huffman Decoder 321. On the other hand, it passes control tokens in parallel. In the Huffman decoder, the Huffman encoded data is decoded in accordance with the first part of the...is set forth in the following sections.

Description of features common to chips in the chip-set:

. Tokens
. Two wire interfaces
. DRAM interface
. Microprocessor interface
. Clocks
. Description of the Spatial Decoder chip
. Description of the Temporal Decoder chip

SECTION A.1

The first description section covers the majority of the electrical...

...2:0
. Flexible chroma sampling formats
. Full JPEG baseline decoding
. Glue-less page mode DRAM interface
. 208 pin PQFP package
. Independent coded data and decoder clocks
. Re-orders MPEG picture sequence

The Video decoder family provides a low chip count solution for implementing high resolution digital video decoders. The chip-set...to control the flow of information. Data is only transferred between blocks when both the sender and receiver are observed to be ready when the clock rises.

1)Data transfer
2)Receiver not ready
3)Sender not ready

If the sender is not ready (as in 3 Sender not ready above...

...PCB tracks between chips. Where possible, track lengths should be kept below 25 mm. The PCB track capacitance should be kept to a minimum.

The clock distribution should be designed to minimize the clock slew between chips. If there is any clock slew, it should be arranged so that "receiving chips" see the clock before "sending chips".1) Note: Figure 38 shows the two-wire interface between the system de-mux chip and the coded data port of the Spatial Decoder operating from the main decoder clock. This is optional as this two wire interface can work from the coded data clock which can be asynchronous to the decoder clock. See Section A.10.5, "Coded data clock". Similarly the display interface of the Image Formatter can operate from a clock that is asynchronous to the main decoder clock.)
1))

All chips communicating via two wire interfaces should operate from the same digital power supply.

A.4.5 Interface timing

A.4.6 - Signal...

...Table A.4.3 are those for V1H)) and V1L)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V.

A.4.7 Control clock

In general, the clock controlling the transfers across the two wire interface is the chip's decoder(underscore)clock. The exception is the coded data port input to the Spatial Decoder. This is controlled by coded(underscore)clock. The clock signals are further described herein.

SECTION A.5 DRAM Interface

A.5.1 The DRAM Interface

A single high performance, configurable, DRAM interface is used... registers of the present invention can be read at any time.

A.5.4 Interface timing (ticks)

The DRAM interface timing is derived from a Clock which is running at four times the input Clock rate of the device (decoder(underscore)clock). This clock is generated by an on-chip PLL.

For brevity, periods of this high speed clock are referred to as

ticks.

A.5.5 Interface registers

A.5.6 Interface operation
The DRAM interface uses fast page mode. Three different types... determined by the register, refresh(underscore)interval.
The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 decoder(underscore)clock cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface to continuously...

...ordinary skill in the art will appreciate that microprocessor interfaces of other widths may also be used. The MPI operates synchronously to various decoder chip clocks,
A.6.1 MPI signals

A.6.2 - MPI electrical specifications

A.6.2.1 AC characteristics

A.6.3 Interrupts
In accordance with the...have no application in the normal use of the devices and need not be accessed by normal device configuration and control software.

SECTION A.7 Clocks
In accordance with the present inventions, many different clocks can be identified in the video decoder system. Examples of clocks are illustrated in Figure 56.
As data passes between different clock regimes within the video decoder chip-set, it is resynchronized (on-chip) to each new clock. In the present invention, the maximum frequency of any input clock is 30 MHz)). However, one of ordinary skill in the art will appreciate that other frequencies, including those greater than 30MHz, may also be used. On each chip, the microprocessor interface (MPI) operates asynchronously to the chip clocks. In addition, the Image Formatter can generate a low frequency audio clock which is synchronous to the decoded video' s picture rate. Accordingly, this clock can be used to provide audio/video synchronization.

A.7.1 Spatial Decoder clock signals
The Spatial Decoder has two different (and potentially asynchronous) clock inputs:

A.7.2 Temporal Decoder clock signals
The Temporal Decoder has only one clock input

A.7.3 Electrical specifications

A.7.3.1 CMOS levels
The clock input signals are CMOS inputs. VIHmin)) is approx. 70% of VDD)) and VILmax)) is approx. 30% of VDD)). The values shown in Table A.7.4 are those for VIH)) and VIL)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V.

A.7.3.2 Stability of clocks

In the present invention, clocks used to drive the DRAM interface and the chip-to-chip interfaces are derived from the input clock signals. The timing specifications for these interfaces assume that the input clock timing is stable to within (+-) 100 ps.

SECTION A.8 JTAG

As circuit boards become more densely populated, it is increasingly difficult to verify the...

...pins. The trst (Test Reset) pin resets the JTAG circuitry, to ensure that the device doesn't power-up in test mode. The tck (Test Clock) pin is used to clock serial test patterns into the tdi (Test Data Input) pin, and out of the tdo (Test Data Output) pin. Lastly, the operational mode of the JTAG circuitry is set by clocking the appropriate sequence of bits into the tms (Test Mode Select) pin.

The JTAG standard is extensible to provide for additional features at the discretion...

...Full JPEG baseline decoding
. Glue-less DRAM interface
. Single +5V supply
. 208 pin PQFP package
. Max. power dissipation 2.5W
. Independent coded data and decoder clocks
. Uses standard page mode DRAM

The Spatial Decoder is a configurable VLSI decoder chip for use in a variety of JPEG. MPEG and H.261...sampled at the same time as data (7:0), coded(underscore)extn and coded(underscore)valid, i.e., on the rising edge of coded(underscore)clock.

A.10.1.2 Byte mode

If, however, byte(underscore)mode is high, then a byte of data is transferred on data(7:0) under...

...Each time before writing to coded(underscore)data(7:0), coded(underscore)busy should be inspected to see if the interface is ready to accept more data.

A.10.3 Switching between input modes

Provided suitable precautions are observed, it is possible to dynamically change the data input mode. In general, the transfer of a Token...

...A. 11). The Start code Detector analyses data in the DATA Tokens bit serially. The Detector's normal rate of processing is one bit per clock cycle (of coded(underscore)clock). Accordingly, it will typically decode a byte of coded data every 8 cycles of coded(underscore) clock. However, extra processing cycles are occasionally required, e.g., when a non-DATA Token is supplied or when a start code is encountered in the...

...buffer newly arriving coded data (or stop new data for arriving) if the Spatial decoder is unable to accept data.

A.10.5 Coded data clock

In accordance with the present invention, the coded data port, the input circuit and other functions in the Spatial Decoder are controlled by coded(underscore)clock. Furthermore, this clock can be asynchronous to the main decoder(underscore)clock. Data transfer is synchronized to decoder(underscore)clock on-chip.

SECTION A.11 Start code detector

A.11.1 Start codes

As is well known in the art, MPEG and H.261 coded... underscore)start(underscore)mask = 0 is recommended to ensure compatibility with future products.

MPEG, on the other hand, was designed to meet the needs of **both** communications (bit **serial**) and computer (byte oriented) systems. Start codes in MPEG data should normally be byte aligned. However, the standard is designed to be allow bit serial...of the buffers ensures that the buffers never empty during decoding and, this, therefore ensures that the decoder is able to decode new pictures at **regular intervals**.

Generally, two facilities are required to correctly start-up a decoder. First, there must be a mechanism to measure how much data has been provided...

...up delay for the first picture, the requirements of all subsequent pictures will be met automatically.

MPEG, therefore, specifies the start-up requirements as a **delay**. However, in a **constant** bit rate system this **delay** can readily be converted to a bit count. This is the basis on which the start-up control of the Spatial Decoder of the present...four main processing blocks in the Video Demux: Parser State Machine, Huffman decoder (including an ITOD), Macroblock counter and ALU.

The Parser or state machine **follows** the syntax of the coded video data and instructs the **other** units. The Huffman decoder **converts** variable length coded (VLC) data into integers. The Macroblock counter keeps track of which section of a picture is being decoded. The ALU performs the...

...SPECIFICATION world, e.g. PAL-NTSC television standards. This is accomplished by selectively dropping or repeating pictures in a manner which is unique. Ordinary "frame rate **converters**," e.g. **2**-3 pulldown, operate with a fixed input picture rate, whereas the Video Formatter can handle a variable input picture rate.

The output rate in terms...

...a spatial decoder may vary in order to interface with various display systems throughout the world, such as NTSC, PAL and SECAM. The video formatter **converts** this variable picture rate to a constant picture rate suitable for display.

The invention is defined in claim 1. Further specific embodiments are defined in...in an exemplifying "data duplication" pipeline stage;

Figures. 9a and 9b taken together depict one example of a timing diagram that shows the two-phase **clock**, the two-wire transfer control signals and the other internal data and control signals used in the exemplifying embodiment shown in Figures. 8a and 8b...

...write timing;

Figure 55 shows organization of large integers in the memory map;

Figure 56 shows a typical decoder dock regime;

Figure 57 shows input **clock** requirements;

Figure 58 shows the Spatial Decoder;

Figure 59 shows the inputs and outputs of the input circuit;

Figure 60 shows the coded port protocol...of pipeline stages.

Furthermore, data may be processed in more than one stage and the processing time for different stages can differ.

In addition to **clock** and data signals (described below), the pipeline includes two transfer control signals -- a "VALID" signal and an "ACCEPT" signal. These signals are used to control...3) illustrate

generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping clock with phases (o slash)0 and (o slash)1. Although a two-phase dock is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a clock with more than two phases.

As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and...

...the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is snown in Fig. 3. A change of state during a clock phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a downward-pointing arrow for changes from HIGH to LOW. Transfer of data from one storage element to another is indicated by a large open arrow. It is assumed that the...

...HIGH whenever the storage elements contain valid data.

In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping clock phases (o slash)0 and (o slash)1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during clock cycle (o slash)1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the clock cycle (o slash)0. Fig. 3 also illustrates that the primary and secondary storage elements in each stage are further connected via an internal acceptance...ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective clock phases until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the ol...

...storage elements (within the same stage or within the preceding pipeline stage). Rather, this change propagates upstream within the pipeline one storage element block per clock phase.

As this example illustrates, the concept of a "stage" in the pipeline structure illustrated in Fig. 3 is to some extent a matter of...process analog signals.

As discussed previously, while other conventional timing arrangements may be used, the interface is preferably controlled by a two-phase, non-overlapping clock. In Figs. 4-9, these clock phase signals are referred to as PH0 and PH1. In Fig. 4, a line is shown for each clock phase signal.

Input data enters a pipeline stage over a multi-bit data bus IN(underscore)DATA and is transferred to a following pipeline stage...

...example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs, that is, they are "loaded", when the clock input is HIGH, i.e., at a logic "1" level. Additionally, the Q outputs hold their last values. In other words, the Q outputs are "latched" on the falling edge of their respective clock signals. Each latch has for its clock either one of two non-overlapping clock signals PH0 or PH1 (as shown in Fig. 5), or the logical AND combination of one of these clock signals PH0, PH1 and one logic signal. The invention works equally well, however, by providing latches that latch on the rising edges of the clock signals, or any other known latching arrangement, as long as conventional methods are applied to ensure proper timing of the latching operations.

The output data...the Q signal and/or its logical inverse.

The data and validation latches LDIN, LDOUT, LVIN and LVOUT, load their respective data inputs when both **clock** signals (PH0 at the input side and PH1 at the output side) and the output from the acceptance latch of the same side are logical "1". Thus, the **clock** signal (PH0 for the input latches LDIN and LVIN) and the output of the respective acceptance latch (in this case, LAIN) are used in a...

...data when either of these two signals goes to a "0".

Although only one of the dock phase signals PH0 or PH1, is used to **clock** the data and validation latches at the input (and output) side of the pipeline stage, the other dock phase signal is used, directly, to dock...signal IN(underscore)VALID to the illustrated stage has not gone to a "1" since the system was most recently reset. Assume further that several **clock** cycles have taken place since the system was last reset and, accordingly, the circuitry has reached a steady-state condition. The validation input signal QVIN from the validation latch LVIN is, therefore, loaded as a "0" during the next positive period of the **clock** PH0. The input to the acceptance input latch LAIN (via the gate NAND1 or another equivalent gate), is, therefore, loaded as a "1" during the...

...transparent latches so that whatever data is on the IN(underscore)DATA bus simply is loaded into the data latch LDIN as soon as the **clock** signal PH0 goes to a "1". Of course, this invalid data will also be loaded into the next data latch LDOUT of the following pipeline...

...by rising to a "1". The output of the corresponding validation latch then rises to a "1" on the next rising edge of its respective **clock** phase signal. For example, the validation input signal QVIN of latch LVIN rises to a "1" when its corresponding IN(underscore)VALID signal goes high (that is, rises to a "1") on the next rising edge of the **clock** phase signal PH0.

Assume now, instead, that the data input latch LDIN contains valid data. If the data output latch LDOUT is ready to accept new data, its acceptance signal QAOUT will be a "1". In this case, during the next positive period of the **clock** signal PH1, the data latch LDOUT and validation latch LVOUT will be enabled, and the data latch LDOUT will load the data present at its input. This will occur before the next rising edge of the other dock signal PH0, since the **clock** signals are non-overlapping. At the next rising edge of PH0, the preceding data latch (LDIN) will, therefore, not latch in new input data from...

...latches (within a stage or between adjacent stages) that are able to accept data, since they will be operating based on alternate phases of the **clock**. Any data latch that is not ready to accept new data because it contains valid data that cannot yet be passed, will have an output...the state of the validation input signal QVIN. The acceptance input signal QAIN then rises to a "1" at the next rising edge of the **clock** signal PH1. Assuming that the validation signal IN(underscore)VALID has been correctly reset to a "0", then upon the subsequent rising edge of the...

...latches in preceding pipeline stages. Indeed, if the reset signal is held low for at least as many full cycles of both phases of the **clock** as there are pipeline stages, it will only be necessary to directly reset the validation output latch in the final pipeline stage.

Figs. 5a and 5b (referred to collectively as Fig. 5) illustrate a timing diagram showing the relationship between the non-overlapping **clock** signals PH0, PH1, the effect of the reset signal, and the holding and transfer of data for the different permutations of validation and acceptance signals...recognize other tokens and passes them on

unaltered. In a large number of cases, only one token is decoded, the DATA Token word itself.

In many applications, the operation of a particular stage will depend upon the results of its own past operations. The "state" of the stage, thus, depends on...

...The value of the extension bit is loaded into LEIN and is then loaded into LEOUT on the next rising edge of the non-overlapping clock phase signal PH1. Latch LEOUT, thus, contains the value of the current extension bit, but only during the second half of the non-overlapping, two-phase clock. Latch LEPREV, however, loads this extension bit value on the next rising edge of the clock signal PHO, that is, the same signal that enables the extension bit input latch LEIN. The output QEPREV of the latch LEPREV, thus, will hold the value of the extension bit during the previous PHO clock phase.

The five bits of the data word output from the inverting Q output, plus the non-inverted MD(2), of the latch LDIN are...of the intermediate extension bit (labeled "MID(underscore)EXTN" and as signal S4), and it loads this value on the next rising edge of the clock phase PHO into the latch LI1, whose output is the bit QI1 and is one of the inputs to the token decoding logic group that...

...the signal DATA(underscore)TOKEN will retain its state (whether "0" or "1"). This is true even though the dock signals PHO and PH1 are clocking the latches (LI2 and LO2 respectively). The value of DATA(underscore)TOKEN can only change when one or both of the signals QI1 and S1...

...NAND22 from the output of NAND20). As a result, this "1" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "1", indicating that the circuitry is processing a DATA token.

The NOT(underscore)DUPLICATE signal (the...states, so that the input latches will be enabled and will be able to accept data, at most, during every other complete cycle of both clock phases PH0, PH1. The additional condition that the following stage be prepared to accept data, as indicated by a "HIGH" OUT(underscore)ACCEPT signal, must, of course, still be satisfied. The output latch LDOUT will, therefore, place the same data word onto the output bus OUT(underscore)DATA for at least two full clock cycles. The OUT(underscore)VALID signal will be a "1" only when there is both a valid DATA(underscore)TOKEN (QO2 HIGH) and the validation...

...is a duplicate (Ql3 is a "O"). If the signal MID(underscore)ACCEPT is HIGH, the latches LO1-LO3 will, therefore, be enabled when the clock signal PH1 is high whenever valid input data is loaded at the input of the stage, or when the latched data is a duplicate.

From...on the downstream latch LVOUT, with the reset signal being propagated backwards to cause the upstream validation latch to be forced low on the next clock cycle.

It should be noted that in the example shown in Fig. 8, the duplication of data contained in DATA tokens serves only as an...I frame to display an interfacent B frame.

Further information will become more readily apparent to one of ordinary skill in the art from the ensuing additional detailed description of illustrative embodiment of the invention which, for purposes of clarity and convenience of explanation are grouped and set forth in the following sections:

1. Multi-Standard Configurations
2. JPEG Still Picture Decoding
3. Motion Picture Decompression

4. RAM Memory Map
5. Bitstream Characteristics
6. Reconfigurable Processing Stage...

...In a first embodiment, in accordance with the present invention, as previously described with reference to Figures 10-12 an address generator is employed to store a block of formatted data, output from either the first decoder (Spatial Decoder) or the combination of the first decoder (Spatial Decoder) and the second...world, e.g. PAL-NTSC television standards. This is accomplished by selectively dropping or repeating pictures in a manner which is unique. Ordinary "frame rate converters," e.g. 2-3 pulldown, operate with a fixed input picture rate, whereas the Video Formatter can handle a variable input picture rate.

6. RECONFIGURABLE PROCESSING STAGE

Referring...tokens are generated by circuitry within the decoder processor and emulate the operation of a number of different type standard-dependent signals passing into the serial pipeline processor for handling. The technique used is to study all the parameters of the multi-standards that are selected for processing by the serial processor and noting 1) their similarities, 2) their dissimilarities, 3) their needs and requirements and 4) selecting the correct token function to effectively process all of the standard signals sent into the carries data from one processing stage to the next. Consequently, the characteristics of this token change as it passes through the decoder. For example, at the input to the Spatial Decoder, DATA Tokens carry bit serial coded video data packed into 8 bit words. Here, there is no limit to the length of each token. However, to illustrate the versatility of...

...construction of both the address generator and the DRAM interface, as discussed further below.

In the present invention, the DRAM Interface can operate from a clock which is asynchronous to both the address generator and to the clocks of the stages through which data is passed. Special techniques have been used to handle this asynchronous nature of the operation.

Data is typically transferred...an address, it waits for the address generator to supply a valid address, processes that address and then sets the accept line high for one clock period. Thus, it implements a request/acknowledge (REQ/ACK) protocol.

A unique feature of the DRAM interface 302 is its ability to communicate independently with...

...control and sends a signal to the read side to indicate that RAM1 is now ready to be read. This signal passes between two asynchronous clock regimes and, therefore, passes through three synchronizing flip flops.

Provided RAM2 312 is empty, the next item of data to arrive on the input side...block in the present Invention uses timing chains to place the edges of the DRAM signals to a precision of a quarter of the system clock period. Two quadrature clocks from the phase locked loop are used. These are combined to form a notional 2x clock. Any one chain is then made from two shift registers in parallel, on opposite phases of the 2x clock.

First of all, there is one chain for the page start cyde and another for the read/write/refresh cycles. The length of each cycle...

...is created. The pulse travels along the chains and is directed by the state information from the DRAM interface. The pulse generates the DRAM interface clock. Each DRAM interface clock period corresponds

to one cycle of the DRAM, consequently, as the DRAM cycles have different lengths, the DRAM interface clock is not at a constant rate.

Moreover, additional timing chains combine the pulse from the above chains with the information from the DRAM interface to...interface (MPI) is used on all circuits with in the Spatial Decoder and Temporal Decoder. The MPI operates asynchronously with various Spatial and Temporal Decoder clocks. Referring to Table A.6.1 of the subsequent further detailed description, there is shown the various MPI signals that are used on this interface:..is set forth in the following sections.

(Description of features common to chips in the chip-set:
(Tokens
(Two wire interfaces
(DRAM interface
(Microprocessor interface
(Clocks
(Description of the Spatial Decoder chip
(Description of the Temporal Decoder chip

SECTION A.1

The first description section covers the majority of the electrical...

...2:0

(Flexible chroma sampling formats
(Full JPEG baseline decoding
(Glue-less page mode DRAM interface
(208 pin PQFP package
(Independent coded data and decoder clocks
(Re-orders MPEG picture sequence

The Video decoder family provides a low chip count solution for implementing high resolution digital video decoders. The chip-set...to control the flow of information. Data is only transferred between blocks when both the sender and receiver are observed to be ready when the clock rises.

1) ...track capacitance should be kept to a minimum.

The dock distribution should be designed to minimize the dock slew between chips. If there is any clock slew, it should be arranged so that "receiving chips" see the clock before "sending chips".1)1)
Note: Figure 38 shows the two-wire interface between the system de-mux chip and the coded data port of the Spatial Decoder operating from the main decoder clock. This is optional as this two wire interface can work from the coded data clock which can be asynchronous to the decoder clock. See Section A.10.5, "Coded data clock".
Similarly the display interface of the Image Formatter can operate from a dock that is asynchronous to the main decoder clock.)

All chips communicating via two wire interfaces should operate from the same digital power supply.

A.4.5 Interface timing

A.4.6 - Signal levels...

...are those for V1H)) and V1L)) at their respective worst case VDD)).
VDD))=5.0(+-)0.25V.

A.4.7 Control dock

In general, the clock controlling the transfers across the two wire interface is the chip's decoder(underscore)clock. The exception is the coded data port input to the Spatial Decoder. This is controlled by coded(underscore)clock. The clock signals are

further described herein.

SECTION A.5 DRAM Interface

A.5.1 The DRAM interface
A single high performance, configurable, DRAM interface is used... registers of the present invention can be read at any time.

A.5.4 Interface timing (ticks)
The DRAM interface timing is derived from a **Clock** which is running at four times the input **Clock** rate of the device (decoder(underscore)**clock**). This dock is generated by an on-chip PLL.
For brevity, periods of this high speed **clock** are referred to as ticks.
A.5.5 Interface registers

A.5.6 Interface operation
The DRAM interface uses fast page mode. Three different types... determined by the register, refresh(underscore)interval.
The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 decoder(underscore)**clock** cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface to continuously...

...ordinary skill in the art will appreciate that microprocessor interfaces of other widths may also be used. The MPI operates synchronously to various decoder chip **clocks**.

A.6.1 MPI signals

A.6.2 - MPI electrical specifications

A.6.2.1 AC characteristics

A.6.3 Interrupts
In accordance with the...have no application in the normal use of the devices and need not be accessed by normal device configuration and control software.

SECTION A.7 **Clocks**
In accordance with the present inventions, many different **clocks** can be identified in the video decoder system. Examples of **clocks** are illustrated in Figure 56.
As data passes between different **clock** regimes within the video decoder chip-set, it is resynchronized (on-chip) to each new **clock**. In the present invention, the maximum frequency of any input **clock** is 30 MHz)). However, one of ordinary skill in the art will appreciate that other frequencies, induding those greater than 30MHz, may also be used. On each chip, the microprocessor interface (MPI) operates asynchronously to the chip docks. In addition, the Image Formatter can generate a low frequency audio **clock** which is synchronous to the decoded video's picture rate. Accordingly, this **clock** can be used to provide audio/video synchronization.
A.7.1 Spatial Decoder **clock** signals
The Spatial Decoder has two different (and potentially asynchronous) dock inputs:

A.7.2 Temporal Decoder dock signals
The Temporal Decoder has only one **clock** input

A.7.3 Electrical specifications

A.7.3.1 CMOS levels
The **clock** input signals are CMOS inputs. VIHmin)) is approx. 70% of VDD)) and VILmax)) is approx. 30% of VDD)). The values shown in Table A.7.4 are those for VIH)) and VIL)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V.

A.7.3.2 Stability of **clocks**
In the present invention, **clocks** used to drive the DRAM interface and the chip-to-chip interfaces are derived from the input dock signals. The timing specifications for these interfaces...

...pins. The trst (Test Reset) pin resets the JTAG circuitry, to ensure that the device doesn't power-up in test mode. The tck (Test **Clock**) pin is used to **clock** serial test patterns into the tdi (Test Data Input) pin, and out of the tdo (Test Data Output) pin. Lastly, the operational mode of the...

...Full JPEG baseline decoding
(Glue-less DRAM interface
(Single +5V supply
(208 pin PQFP package
(Max. power dissipation 2.5W
(Independent coded data and decoder **clocks**
(Uses standard page mode DRAM
The Spatial Decoder is a configurable VLSI decoder chip for use in a variety of JPEG, MPEG and H.261...sampled at the same time as data (7:0), coded(underscore)extn and coded(underscore)valid, i.e., on the rising edge of coded(underscore)**clock**.

A.10.1.2 Byte mode
If, however, byte(underscore)mode is high, then a byte of data is transferred on data(7:0) under...

...Token header to be generated on-chip. Any further bytes transferred in byte mode are thereafter appended to this DATA Token until the input mode **changes**. Recall, DATA Tokens can contain as many bits as are necessary.
The MPI register bit, coded busy, and the signal, coded(underscore)accept, indicate on...

...A.11). The Start code Detector analyses data in the DATA Tokens bit serially. The Detector's normal rate of processing is one bit per **clock** cycle (of coded(underscore)**clock**). Accordingly, it will typically decode a byte of coded data every 8 cycles of coded(underscore)dock However, extra processing cycles are occasionally required, e...

...buffer newly arriving coded data (or stop new data for arriving) if the Spatial decoder is unable to accept data.

A.10.5 Coded data **clock**
In accordance with the present invention, the coded data port, the input circuit and other functions in the Spatial Decoder are controlled by coded(underscore)**clock**. Furthermore, this dock can be

asynchronous to the main decoder(underscore)clock. Data transfer is synchronized to decoder(underscore)clock on-chip.

SECTION A.11 Start code detector

A.11.1 Start codes

As is well known in the art, MPEG and H.261 coded...the start-up of the decoder.

A.11.2 Start code detector registers

As previously discussed, many of the Start Code Detector registers are in constant use by the Start Code Detector. So, accessing these registers will be unreliable if the Start Code Detector is processing data. The user is responsible...of the buffers ensures that the buffers never empty during decoding and, this, therefore ensures that the decoder is able to decode new pictures at regular intervals.

Generally, two facilities are required to correctly start-up a decoder. First, there must be a mechanism to measure how much data has been provided...

...up delay for the first picture, the requirements of all subsequent pictures will be met automatically.

MPEG, therefore, specifies the start-up requirements as a delay. However, in a constant bit rate system this delay can readily be converted to a bit count. This is the basis on which the start-up control of the Spatial Decoder of the present...four main processing blocks in the Video Demux: Parser State Machine, Huffman decoder (including an ITOD), Macroblock counter and ALU.

The Parser or state machine follows the syntax of the coded video data and instructs the other units. The Huffman decoder converts variable length coded (VLC) datainto integers. The Macroblock counter keeps track of which section of a picture is being decoded. The ALU performs the necessary...buffer verifier buffer size

If any of these parameters change when the Spatial Decoder decodes a sequence header, the Parser event ERR(underscore)MPEG(underscore) SEQUENCE will be generated.

A.14.8.1 Change in picture size

If the picture size has changed, the user's software should read the values in horiz(underscore)pels and vert(underscore)pels and compute new values to be loaded into the...also be decoded. However, some reconfiguration between scans may be required to accomodate the next set of components to be decoded.

A.16.2 Token sequence

The JPEG markers codes are converted to an analogous MPEG named Token by the Start Code Detector (see Table A.11.4, see Fig. 82 "Tokenized JPEG picture").

SECTION A.17...

...4:2:0 MPEG video can be decoded.

The Temporal Decoder is not required for Intra coding schemes (such as JPEG). If induded in a multi-standard decoder, the Temporal Decoder will pass decoded JPEG pictures through to its output.

Note: The above values are merely illustrative, by way of example...

...CLAIMS universal adaptation units for interfacing with said stages and interacting with selected stages, said two-wire interfaces each comprising :

a sender,
a receiver, and
a **clock** connected to said sender and said receiver, said **clock** having transitions from
a first state to a second state,

wherein data is transferred from said sender to said receiver upon a **clock** transition only when said sender is ready and said receiver is ready;

said processing stages comprising an image formatter receiving said tokens via a first...

...CLAIMS for each of a VALID transfer control signal and an ACCEPT transfer control signal respectively, said two-wire interface comprising a sender, a receiver, a **clock** connected to said sender and said receiver, said **clock** having transitions from a first state to a second state, wherein data is transferred from said sender to said receiver upon a **clock** transition only when said sender is ready and said receiver is ready;
each of said control and/or DATA tokens being a universal adaptation unit...

37/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00975324
Pipeline decoding system
Pipeline-System zur Dekodierung
Systeme pipeline de decodage
PATENT ASSIGNEE:
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PATENT (CC, No, Kind, Date): EP 884910 A1 981216 (Basic)
EP 884910 B1 010509
APPLICATION (CC, No, Date): EP 98202132 950228;
PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
RELATED PARENT NUMBER(S) - PN (AN):
EP 674443 (EP 95301301)
INTERNATIONAL PATENT CLASS (V7): H04N-007/24; G06F-013/00; G06F-009/38
ABSTRACT WORD COUNT: 104
NOTE:
Figure number on first page: 76

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199851	498
CLAIMS B	(English)	200119	330
CLAIMS B	(German)	200119	308
CLAIMS B	(French)	200119	382
SPEC A	(English)	199851	126705
SPEC B	(English)	200119	122739

Total word count - document A 127222
Total word count - document B 123759
Total word count - documents A + B 250981

...SPECIFICATION Token header to be generated on-chip. Any further bytes transferred in byte mode are thereafter appended to this DATA Token until the input mode **changes**. Recall, DATA Tokens can contain as many bits as are necessary.

The MPI register bit, coded busy, and the signal, coded(underscore)accept, indicate on...

...A.11). The Start code Detector analyses data in the DATA Tokens bit serially. The Detector's normal rate of processing is one bit per **clock** cycle (of coded(underscore)**clock**). Accordingly, it will typically decode a byte of coded data every 8 cycles of coded(underscore) **clock**. However, extra processing cycles are occasionally required, e.g., when a non-DATA Token is supplied or when a start code is encountered in the...

...buffer newly arriving coded data (or stop new data for arriving) if the Spatial decoder is unable to accept data.

A.10.5 Coded data **clock**

In accordance with the present invention, the coded data port, the input circuit and other functions in the Spatial Decoder are controlled by coded(underscore)**clock**. Furthermore, this **clock** can be asynchronous to the main decoder(underscore)**clock**. Data transfer is synchronized to decoder(underscore)**clock** on-chip.

SECTION A.11 Start code detector

A.11.1 Start codes

...the start-up of the decoder.

A.11.2 Start code detector registers

As previously discussed, many of the Start Code Detector registers are in **constant** use by the Start Code Detector. So, accessing these registers will be unreliable if the Start Code Detector is processing data. The user is responsible...of the buffers ensures that the buffers never empty during decoding and, this, therefore ensures that the decoder is able to decode new pictures at **regular intervals**.

Generally, two facilities are required to correctly start-up a decoder. First, there must be a mechanism to measure how much, data has been provided...

...up delay for the first picture, the requirements of all subsequent pictures will be met automatically.

MPEG, therefore, specifies the start-up requirements as a **delay**. However, in a **constant** bit rate system this **delay** can readily be converted to a bit count. This is the basis on which the start-up control of the Spatial Decoder of the present...four main processing blocks in the Video Demux: Parser State Machine, Huffman decoder (including an ITOD), Macroblock counter and ALU.

The Parser or state machine **follows** the syntax of the ceded video data and instructs the **other** units. The Huffman decoder **converts** variable length coded (VLC) data into integers. The Macroblock counter keeps track of which section of a picture is being decoded. The ALU performs the...

37/3,K/12 (Item 12 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00711605
Reconfigurable data processing stage

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PATENT (CC, No, Kind, Date): EP 674446 A2 950927 (Basic)
EP 674446 A3 960814
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PRIORITY (CC, No, Date): GB 9405914 940324
DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; IT; LI; NL
INTERNATIONAL PATENT CLASS (V7): H04N-007/24; G06F-013/00; G06F-009/38
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CLAIMS A (English) EPAB95 2475
CLAIMS B (English) 200131 1079
CLAIMS B (German) 200131 1072
CLAIMS B (French) 200131 1186
SPEC A (English) EPAB95 125236
SPEC B (English) 200131 121335
Total word count - document A 127738
Total word count - document B 124672
Total word count - documents A + B 252410

...SPECIFICATION field of image data samples to provide for one or more of the functions of decimation, interpolation, and sharpening. This is accomplished by an array **transform** processor such as that employed in a JPEG compression system. Blocks of data samples are transformed by the discrete even cosine transform (DECT) in both...

...the proposed ISO/IEC MPEG standards. Included are three cooperating components or subsystems that operate to variously adaptively pre-process the incoming digital motion video **sequences**, allocate bits to the

pictures in a **sequence**, and adaptively quantize **transform** coefficients in **different** regions of a picture in a video **sequence** so as to provide optimal visual quality given the number of bits allocated to that picture.

United States Patent No. 5,267,334 discloses a...following the first image in time in the sequence of moving images. This at least one frame being known as an interframe. Finally, detecting a **second** scene **change** in the **sequence** of moving images and generating a second keyframe containing complete scene information for an image displayed at the time just prior to the **second** scene **change**, known as a "backward-facing" keyframe. The first keyframe and the at least one intermediate compressed frame are linked for forward play, and the second...2) illustrate the control of data transfer between stages of a preferred embodiment of a pipeline using a two-wire interface and a multi-phase **clock**;

Figure. 4 is a block diagram that illustrates a basic embodiment of a pipeline stage that incorporates a two-wire transfer control and also shows...

...in an exemplifying "data duplication" pipeline stage;

Figures. 9a and 9b taken together depict one example of a timing diagram that shows the two-phase **clock**, the two-wire transfer control signals and the other internal data and control signals used in the exemplifying embodiment shown in Figures. 8a and 8b...

...shows a macroblock structure;

Figure 37 shows a two-wire interface protocol;
Figure 38 shows the location of external two-wire interfaces;
Figure 39 shows **clock** propagation;
Figure 40 shows two-wire interface timing;
Figure 41 shows examples of access structure;
Figure 42 shows a read transfer cycle;
Figure 43 shows...

...timing;

Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory map;
Figure 56 shows a typical decoder **clock** regime;
Figure 57 shows input **clock** requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit;
Figure 60 shows the coded port protocol...of pipeline stages.

Furthermore, data may be processed in more than one stage and the processing time for different stages can differ.

In addition to **clock** and data signals (described below), the pipeline includes two transfer control signals -- a "VALID" signal and an "ACCEPT" signal. These signals are used to control...3) illustrate generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping **clock** with phases o0 and o1. Although a two-phase **clock** is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a **clock** with more than two phases.

As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and...

...the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is snown in Fig. 3. A change of state during a **clock** phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a

...

...HIGH whenever the storage elements contain valid data.

In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping clock phases o0 and o1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during clock cycle o1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the clock cycle o0. Fig. 3 also illustrates that the primary and secondary storage elements in each stage are further connected via an internal acceptance line to...

...ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective clock phases until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the o1...storage elements (within the same stage or within the preceding pipeline stage). Rather, this change propagates upstream within the pipeline one storage element block per clock phase.

As this example illustrates, the concept of a "stage" in the pipeline structure illustrated in Fig. 3 is to some extent a matter of...

...signal LOW not only when all of the downstream storage elements are filled with valid data, but also when a stage requires more than one clock phase to finish processing its data. This also can occur when it creates valid data in one or both of its storage elements. In other... process analog signals.

As discussed previously, while other conventional timing arrangements may be used, the interface is preferably controlled by a two-phase, non-overlapping clock. In Figs. 4-9, these clock phase signals are referred to as PH0 and PH1. In Fig. 4, a line is shown for each clock phase signal.

Input data enters a pipeline stage over a multi-bit data bus IN...

...example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs, that is, they are "loaded", when the clock input is HIGH, i.e., at a logic "1" level. Additionally, the Q outputs hold their last values. In other words, the Q outputs are "latched" on the falling edge of their respective clock signals. Each latch has for its clock either one of two non-overlapping clock signals PH0 or PH1 (as shown in Fig. 5), or the logical AND combination of one of these clock signals PH0, PH1 and one logic signal. The invention works equally well, however, by providing latches that latch on the rising edges of the clock signals, or any other known latching arrangement, as long as conventional methods are applied to ensure proper timing of the latching operations.

The output data...the Q signal and/or its logical inverse.

The data and validation latches LDIN, LDOUT, LVIN and LVOUT, load their respective data inputs when both clock signals (PH0 at the input side and PH1 at the output side) and the output from the acceptance latch of the same side are logical "1". Thus, the clock signal (PH0 for the input latches LDIN and LVIN) and the output of the respective acceptance latch (in this case, LAIN) are used in a...

...and QAIN are both "1". It will latch this data when either of these two signals goes to a "0".

Although only one of the clock phase signals PH0 or PH1, is used to clock the data and validation latches at the input (and output) side of the pipeline stage, the other clock phase signal is used, directly, to clock the acceptance latch at the same side. In other

words, the acceptance latch on either side (input or output) of a pipeline stage is preferably clocked "out of phase" with the data and validation latches on the same side. For example, PH1 is used to clock the acceptance input latch, although PH0 is used in generating the clock signal CK for the data latch LDIN and the validation latch LVIN.

As an example of the operation of a pipeline augmented by the two...

...VALID to the illustrated stage has not gone to a "1" since the system was most recently reset. Assume further that several clock cycles have taken place since the system was last reset and, accordingly, the circuitry has reached a steady-state condition. The validation input signal QVIN from the validation latch LVIN is, therefore, loaded as a "0" during the next positive period of the clock PH0. The input to the acceptance Input latch LAIN (via the gate NAND1 or another equivalent gate), is, therefore, loaded as a "1" during the next positive period of the clock signal PH1. In other words, since the data in the data input latch LDIN is not valid, the stage signals that it is ready to...

...DATA bus simply is loaded into the data latch LDIN as soon as the clock signal PH0 goes to a "1". Of course, this invalid data will also be loaded into the next data latch LDOUT of the following pipeline ...

...a data latch does not contain valid data, it accepts or "loads" any data presented to it during the next positive period of its respective clock signal. On the other hand, such invalid data is not loaded in any stage for which the acceptance signal from its corresponding acceptance latch is...

...by rising to a "1". The output of the corresponding validation latch then rises to a "1" on the next rising edge of its respective clock phase signal. For example, the validation input signal QVIN of latch LVIN rises to a "1" when its corresponding IN...

...VALID signal goes high (that is, rises to a "1") on the next rising edge of the clock phase signal PH0.

Assume now, instead, that the data input latch LDIN contains valid data. If the data output latch LDOUT is ready to accept new data, its acceptance signal QAOUT will be a "1". In this case, during the next positive period of the clock signal PH1, the data latch LDOUT and validation latch LVOUT will be enabled, and the data latch LDOUT will load the data present at its input. This will occur before the next rising edge of the other clock signal PH0, since the clock signals are non-overlapping. At the next rising ...latches (within a stage or between adjacent stages) that are able to accept data, since they will be operating based on alternate phases of the clock. Any data latch that is not ready to accept new data because it contains valid data that cannot yet be passed, will have an output...

...the state of the validation input signal QVIN. The acceptance input signal QAIN then rises to a "1" at the next rising edge of the clock signal PH1. Assuming that the validation signal IN...

...VALID has been correctly reset to a "0", then upon the subsequent rising edge of the clock signal PH0, the output from the validation latch LVIN will become a "0", as it would have done if it had been reset directly.

As...

...latch: If the reset signal NOTRESET0 can be guaranteed to be low during

more than one complete cycle of both phases PH0, PH1 of the clock, then the "automatic reset" (a backwards propagation of the reset signal) will occur for validation latches in preceding pipeline stages. Indeed, if the reset signal is held low for at least as many full cycles of both phases of the clock as there are pipeline stages, it will only be necessary to directly reset the validation output latch in the final pipeline stage.

Figs. 5a and 5b (referred to collectively as Fig. 5) illustrate a timing diagram showing the relationship between the non-overlapping clock signals PH0, PH1, the effect of the reset signal, and the holding and transfer of data for the different permutations of validation and acceptance signals into and between the two illustrated sides of a pipeline stage configured in the embodiment shown in Fig. 4... recognize other tokens and passes them on unaltered. In a large number of cases, only one token is decoded, the DATA Token word itself.

In many applications, the operation of a particular stage will depend upon the results of its own past operations. The "state" of the stage, thus, depends on its previous states. In other words, the stage depends upon stored state information, which is another way of saying it must retain some information about its own history one or more clock cycles ago. The present invention is well-suited for use in pipelines that include such "state machine" stages, as well as for use in applications...The value of the extension bit is loaded into LEIN and is then loaded into LEOUT on the next rising edge of the non-overlapping clock phase signal PH1. Latch LEOUT, thus, contains the value of the current extension bit, but only during the second half of the non-overlapping, two-phase clock. Latch LEPREV, however, loads this extension bit value on the next rising edge of the clock signal PHO, that is, the same signal that enables the extension bit input latch LEIN. The output QEPREV of the latch LEPREV, thus, will hold the value of the extension bit during the previous PHO clock phase.

The five bits of the data word output from the inverting Q output, plus the non-inverted MD(2), of the latch LDIN are...of the extension bit at the input and at the output of the stage, respectively. As Fig. 8a shows, the input extension latch LEIN is clocked synchronously with the input data latch LDIN and the validation signal IN EXTN" and as signal S4), and it loads this value on the next rising edge of the clock phase PHO into the latch LI1, whose output is the bit QI1 and is one of the inputs to the token decoding logic group that...

...TOKEN will retain its state (whether "0" or "1"). This is true even though the clock signals PHO and PH1 are clocking the latches (LI2 and LO2 respectively). The value of DATA...

...S2 will thus be a "0". As a result, this "0" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA ... NAND22 from the output of NAND20). As a result, this "1" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA...

...DUPLICATE signal (the output signal QO3) is similarly loaded into the latch LI3 on the next rising edge of the clock PHO. The output signal QI3 from the latch LI3 is combined with the output signal QI2 in a gate NAND24 to form the signal S3...

...is not a duplicate (QI3 = 0), then the signal S3 goes high.

Assume now, that the DATA TOKEN signal remains HIGH for more than one clock signal. Since the NOT...states, so that the input latches will be enabled and will be able to accept data, at most, during every other complete cycle of both clock phases PH0, PH1. The additional condition that the following stage be prepared to accept data, as

indicated by a "HIGH" OUT...

...DATA for at least two full **clock** cycles. The OUT...ACCEPT is HIGH, the latches LO1-LO3 will, therefore, be enabled when the **clock** signal PH1 is high whenever valid input data is loaded at the input of the stage, or when the latched data is a duplicate.

From...

...on the downstream latch LVOUT, with the reset signal being propagated backwards to cause the upstream validation latch to be forced low on the next **clock** cycle.

It should be noted that in the example shown in Fig. 8, the duplication of data contained in DATA tokens serves ...timing diagram for the data duplication circuit shown in Figs. 8a and 8b. As before, the timing diagram shows the relationship between the two-phase **clock** signals, the various internal and external control signals, and the manner in which data is **clocked** between the input and output sides of the stage and is duplicated.

Referring now more particularly to Figure 10, there is shown a reconfigurable process The output from the prediction filter 103 is passed over line 104 as a **second** input to the summer 98. A first output from the summer 98 is passed over line 105 to output selector 106. A second output from...detecting the presence of a start code image, the detector 225 transmits a start image over a line 227 to a value decoder 228.

A **second** output from the decode register 224 is passed **serially** over line 229 to a value decode shift register 230. The value decode shift register 230 can hold a data value image fifteen bits long...

...bits at a time. While 15 bits has been chosen here as the width in the present invention it will be appreciated that bits of **other** lengths may also be used. The index-to-tokens **converter** 234 **converts** the information to token images using a second look-up table (not shown) similar to that given in Table 12-3 of the Users Manual...difference is the program in the microcode for each of the standards. Thus, when operating in H.261, one program is running, and when a **different** program is running, there is no overlap between them. The same holds true for JPEG, which is a third, completely independent program.

The next unit is the Huffman decoder 56 which functions with the index to data unit 64. Those **two** units cooperate together to perform the Huffman decoding. Here, the algorithm that is used for Huffman decoding is the same, irrespective of the compression standard...

...parser state machine operates with a different program for each of the three compression standards and issues the correct command to the Huffman decoder at **different** times consistent with the standard in operation.

The last unit on the chip that is dependent on the compression standard is the inverse quantizer 79...sequence of pictures may have a totally different picture size and, hence, have a different length when compared to the first length. Again, all such **second** **sequence** of similar pictures are of the same length in bits by the time such pictures reach the output of the Spatial Decoder.

Another aspect of...encoded signals, larger logic DRAM buffers may be required to support the larger picture formats possible with MPEG.

The picture information is moving through the **serial** pipeline in 8 pel by 8 pel blocks. In one form of the invention, the address decoding circuitry handles these pel blocks (storing and retrieving...hereinafter in the section on flushing. In brief, the Spatial Decoder can provide a fake I or P picture at the end of a video **sequence** to flush out the

last P or I picture. In turn, this fake picture is flushed when a subsequent video sequence starts.

The peak memory...when it is appropriate for this to occur. On many occasions, a control token arrives first, reconfigures the action identification circuit 39 and is immediately **followed** by a DATA token which is then processed by the processing unit 36. The control token exits the output latches circuit 41 over the output...START token. In a similar way, the MPEG **sequence** ...construction of both the address generator and the DRAM interface, as discussed further below.

In the present invention, the DRAM interface can operate from a **clock** which is asynchronous to both the address generator and to the **clocks** of the stages through which data is passed. Special techniques have been used to handle this asynchronous nature of the operation.

Data is typically transferred...

...an address, it waits for the address generator to supply a valid address, processes that address and then sets the accept line high for one **clock** period. Thus, it implements a request/acknowledge (REQ/ACK) protocol.

A unique feature of the DRAM interface 302 is its ability to communicate independently with...control and sends a signal to the read side to indicate that RAM1 is now ready to be read. This signal passes between two asynchronous **clock** regimes and, therefore, passes through three synchronizing flip flops.

Provided RAM2 312 is empty, the next item of data to arrive on the input side...block in the present invention uses timing chains to place the edges of the DRAM signals to a precision of a quarter of the system **clock** period. Two quadrature **clocks** from the phase locked loop are used. These are combined to form a notional 2x **clock**. Any one chain is then made from two shift registers in parallel, on opposite phases of the 2x **clock**.

First of all, there is one chain for the page start cycle and another for the read/write/refresh cycles. The length of each cycle...

...is created. The pulse travels along the chains and is directed by the state information from the DRAM interface. The pulse generates the DRAM interface **clock**. Each DRAM interface **clock** period corresponds to one cycle of the DRAM, consequently, as the DRAM cycles have different lengths, the DRAM interface **clock** is not at a constant rate.

Moreover, additional timing chains combine the pulse from the above chains with the information from the DRAM interface to...

...interface (MPI) is used on all circuits with in the Spatial Decoder and Temporal Decoder. The MPI operates asynchronously with various Spatial and Temporal Decoder **clocks**. Referring to Table A.6.1 of the subsequent further detailed description, there is shown the various MPI signals that are used on this interface...however, that, other images from other data bitstreams can be used for this purpose. Accordingly, these images can be used throughout this present invention to **change** it to **another** embodiment which is capable of using the combination of control tokens, and DATA tokens along with the reconfiguration circuits, to provide similar processing.

The use...is set forth in the following sections.

Description of features common to chips in the chip-set:

Tokens

Two wire interfaces

DRAM interface

Microprocessor interface

Clocks

Description of the Spatial Decoder chip

Description of the Temporal Decoder chip

SECTION A.1

The first description section covers the majority of the electrical...

...2:0

Flexible chroma sampling formats

Full JPEG baseline decoding

Glue-less page mode DRAM interface

208 pin PQFP package

Independent coded data and decoder **clocks**

Re-orders MPEG picture sequence

The Video decoder family provides a low chip count solution for implementing high resolution digital video decoders. The chip-set...to control the flow of information.

Data is only transferred between blocks when both the sender and receiver are observed to be ready when the **clock** rises.

1)Data transfer

2)Receiver not ready

3)Sender not ready

If the sender is not ready (as in 3 Sender not ready above...PCB tracks between chips. Where possible, track lengths should be kept below 25 mm. The PCB track capacitance should be kept to a minimum.

The **clock** distribution should be designed to minimize the **clock** slow between chips. If there is any **clock** slew, it should be arranged so that "receiving chips" see the **clock** before "sending chips".(sup 1)

(Footnote: (sup 1) Note: Figure 38 shows the two-wire interface between the system de-mux chip and the coded data port of the Spatial Decoder operating from the main decoder **clock**. This is optional as this two wire interface can work from the coded data **clock** which can be asynchronous to the decoder **clock**. See Section A.10.5, "Coded data **clock**". Similarly the display interface of the Image Formatter can operate from a **clock** that is asynchronous to the main decoder **clock**.)

All chips communicating via two wire interfaces should operate from the same digital power supply.

A.4.5 Interface timing (see image in original document...

...1L)) at their respective worst case V(sub(DD)). V(sub(DD))=5.0(+-)0.25V. (see image in original document)

A.4.7 Control **clock**

In general, the **clock** controlling the transfers across the two wire interface is the chip's decoder...

...**clock**. The exception is the coded data port input to the Spatial Decoder. This is controlled by coded...

...**clock**. The **clock** signals are further described herein.

SECTION A.5 DRAM Interface

A.5.1 The DRAM interface

A single high performance, configurable, DRAM interface is used... registers of the present invention can be read at any time.

A.5.4 Interface timing (ticks)

The DRAM interface timing is derived from a **Clock** which is running at four times the input **Clock** rate of the device (decoder ...

...**clock**). This **clock** is generated by an on-chip PLL.

For brevity, periods of this high speed **clock** are referred to as ticks.

A.5.5 Interface registers (see image in original document) (see image in

original document)
A.5.6 Interface operation...clock cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface to continuously...ordinary skill in the art will appreciate that microprocessor interfaces of other widths may also be used. The MPI operates synchronously to various decoder chip clocks.
A.6.1 MPI signals
(Table omitted)
A.6.2 MPI electrical specifications (see image in original document) (see image in original document) (see image...

...SPECIFICATION shows a macroblock structure;
Figure 37 shows a two-wire interface protocol:
Figure 38 shows the location of external two-wire interfaces;
Figure 39 shows clock propagation;
Figure 40 shows two-wire interface timing:
Figure 41 shows examples of access structure:
Figure 42 shows a read transfer cycle;
Figure 43 shows...

...timing;
Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory map;
Figure 56 shows a typical decoder clock regime;
Figure 57 shows input clock requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit;
Figure 60 shows the coded port protocol...of pipeline stages.
Furthermore, data may be processed in more than one stage and the processing time for different stages can differ.
In addition to clock and data signals (described below), the pipeline includes two transfer control signals -- a "VALID" signal and an "ACCEPT" signal. These signals are used to control...3) illustrate generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping clock with phases (o slash)0 and (o slash)1. Although a two-phase clock is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a clock with more than two phases.
As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and...

...the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is snown in Fig. 3. A change of state during a clock phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a ...

...HIGH whenever the storage elements contain valid data.
In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping clock phases (o slash)0 and (o slash)1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during clock cycle (o slash)1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the clock cycle (o slash)0. Fig. 3 also illustrates that the primary and secondary ...ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective clock phases

until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the (o... storage elements (within the same stage or within the preceding pipeline stage). Rather, this change propagates upstream within the pipeline one storage element block per clock phase.

As this example illustrates, the concept of a "stage" in the pipeline structure illustrated in Fig. 3 is to some extent a matter of...

...signal LOW not only when all of the downstream storage elements are filled with valid data, but also when a stage requires more than one clock phase to finish processing its data. This also can occur when it creates valid data in one or both of its storage elements. In other...

...process analog signals.

As discussed previously, while other conventional timing arrangements may be used, the interface is preferably controlled by a two-phase, non-overlapping clock. In Figs. 4-9, these clock phase signals are referred to as PH0 and PH1. In Fig. 4, a line is shown for each clock phase signal.

Input data enters a pipeline stage over a multi-bit data bus IN(underscore)DATA and is transferred to a following pipeline stage... example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs, that is, they are "loaded", when the clock input is HIGH, i.e., at a logic "1" level. Additionally, the Q outputs hold their last values. In other words, the Q outputs are "latched" on the falling edge of their respective clock signals. Each latch has for its clock either one of two non-overlapping clock signals PH0 or PH1 (as shown in Fig. 5), or the logical AND combination of one of these clock signals PH0, PH1 and one logic signal. The invention works equally well, however, by providing latches that latch on the rising edges of the clock signals, or any other known latching arrangement, as long as conventional methods are applied to ensure proper timing of the latching operations.

The output data...the Q signal and/or its logical inverse.

The data and validation latches LDIN, LDOUT, LVIN and LVOUT, load their respective data inputs when both clock signals (PHO at the input side and PH1 at the output side) and the output from the acceptance latch of the same side are logical "1". Thus, the clock signal (PH0 for the input latches LDIN and LVIN) and the output of the respective acceptance latch (in this case, LAIN) are used in a...

...and QAIN are both "1". It will latch this data when either of these two signals goes to a "0".

Although only one of the clock phase signals PH0 or PH1, is used to clock the data and validation latches at the input (and output) side of the pipeline stage, the other clock phase signal is used, directly, to clock the acceptance latch at the same side. In other words, the acceptance latch on either side (input or output) of a pipeline stage is preferably clocked "out of phase" with the data and validation latches on the same side. For example, PH1 is used to clock the acceptance input latch, although PH0 is used in generating the clock signal CK for the data latch LDIN and the validation latch LVIN.

As an example of the operation of a pipeline augmented by the two...

...signal IN(underscore)VALID to the illustrated stage has not gone to a "1" since the system was most recently reset. Assume further that several clock cycles have taken place since the system was last reset and, accordingly, the circuitry has reached a steady-state condition. The validation input signal QVIN from the validation latch LVIN is, therefore, loaded as a "0" during the next positive period of the

clock PH0. The input to the acceptance input latch LAIN (via the gate NAND1 or another equivalent gate), is, therefore, loaded as a "1" during the next positive period of the clock signal PH1. In other words, since the data in the data input latch LDIN is not valid, the stage signals that it is ready to...

...transparent latches so that whatever data is on the IN(underscore)DATA bus simply is loaded into the data latch LDIN as soon as the clock signal PHO goes to a "1". Of course, this invalid data will also be loaded into the next data latch LDOUT of the following pipeline...

...a data latch does not contain valid data, it accepts or "loads" any data presented to it during the next positive period of its respective clock signal. On the other hand, such invalid data is not loaded in any stage for which the acceptance signal from its corresponding acceptance latch is...

...by rising to a "1". The output of the corresponding validation latch then rises to a "1" on the next rising edge of its respective clock phase signal. For example, the validation input signal QVIN of latch LVIN rises to a "1" when its corresponding IN(underscore)VALID signal goes high (that is, rises to a "1") on the next rising edge of the clock phase signal PH0.

Assume now, instead, that the data input latch LDIN contains valid data. If the data output latch LDOUT is ready to accept new data, its acceptance signal QAOUT will be a "1". In this case, during the next positive period of the clock signal PH1, the data latch LDOUT and validation latch LVOUT will be enabled, and the data latch LDOUT will load the data present at its input. This will occur before the next rising edge of the other clock signal PH0, since the clock signals are non-overlapping. At the next rising edge of PH0, the preceding data latch (LDIN) will, therefore, not latch in new input data from on alternate phases of the clock. Any data latch that is not ready to accept new data because it contains valid data that cannot yet be passed, will have an output...

...the state of the validation input signal QVIN. The acceptance input signal QAIN then rises to a "1" at the next rising edge of the clock signal PH1. Assuming that the validation signal IN(underscore)VALID has been correctly reset to a "0", then upon the subsequent rising edge of the clock signal PH0, the output from the validation latch LVIN will become a "0", as it would have done if it had been reset directly.

As...

...latch: If the reset signal NOTRESET0 can be guaranteed to be low during more than one complete cycle of both phases PH0, PH1 of the clock, then the "automatic reset" (a backwards propagation of the reset signal) will occur for validation latches in preceding pipeline stages. Indeed, if the reset signal is held low for at least as many full cycles of both phases of the clock as there are pipeline stages, it will only be necessary to directly reset the validation output latch in the final pipeline stage.

Figs. 5a and 5b (referred to collectively as Fig. 5) illustrate a timing diagram showing the relationship between the non-overlapping clock signals PH0, PH1, the effect of the reset signal, and the holding and transfer of data for the different permutations of validation and acceptance signals...a particular stage will depend upon the results of its own past operations. The "state" of the stage, thus, depends on its previous states. In other words, the stage depends upon stored state information, which is another way of saying it must retain some

information about its own history one or more clock cycles ago. The present invention is well-suited for use in pipelines that include such "state machine" stages, as well as for use in applications...

...The value of the extension bit is loaded into LEIN and is then loaded into LEOUT on the next rising edge of the non-overlapping clock phase signal PH1. Latch LEOUT, thus, contains the value of the current extension bit, but only during the second half of the non-overlapping, two-phase clock. Latch LEPREV, however, loads this extension bit value on the next rising edge of the clock signal PHO, that is, the same signal that enables the extension bit input latch LEIN. The output QEPREV of the latch LEPREV, thus, will hold the value of the extension bit during the previous PHO clock phase.

The five bits of the data word output from the inverting Q output, plus the non-inverted MD(2), of the latch LDIN are...of the extension bit at the input and at the output of the stage, respectively. As Fig. 8a shows, the input extension latch LEIN is clocked synchronously with the input data latch LDIN and the validation signal IN(underscore)VALID.

In the duplication stage, the output from the data latch LDIN...

...of the intermediate extension bit (labeled "MID(underscore)EXTN" and as signal S4), and it loads this value on the next rising edge of the clock phase PHO into the latch LI1, whose output is the bit QI1 and is one of the inputs to the token decoding logic group that...

...both QI1 and S1 are HIGH, the signal DATA(underscore)TOKEN will retain its state (whether "0" or "1"). This is true even though the clock signals PHO and PH1 are clocking the latches (LI2 and LO2 respectively). The value of DATA(underscore)TOKEN can only change when one or both of the signals QI1 and S1...S2 will thus be a "0". As a result, this "0" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "0", indicating that the circuitry is not processing a DATA token.

If QI1 is "0" and...

...NAND22 from the output of NAND20). As a result, this "1" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "1", indicating that the circuitry is processing a DATA token.

The NOT(underscore)DUPLICATE signal (the output signal QO3) is similarly loaded into the latch LI3 on the next rising edge of the clock PHO. The output signal QI3 from the latch LI3 is combined with the output signal QI2 in a gate NAND24 to form the signal S3...

...is not a duplicate (QI3 = 0), then the signal S3 goes high.

Assume now, that the DATA TOKEN signal remains HIGH for more than one clock signal. Since the NOT(underscore)DUPLICATE signal (QO3) is "fed back" to the latch LI3 and will be inverted by the gate NAND 24 (since...

...states, so that the input latches will be enabled and will be able to accept data, at most, during every other complete cycle of both clock phases PH0, PH1. The additional condition that the following stage be prepared to accept data, as indicated by a "HIGH" OUT(underscore)ACCEPT signal, must...

...course, still be satisfied. The output latch LDOUT will, therefore, place the same data word onto the output bus OUT(underscore)DATA for at least two full clock cycles. The OUT(underscore)VALID signal will be a "1" only when there is both a valid DATA(underscore)TOKEN (QO2 HIGH) and the validation...is a duplicate (QI3 is a "O"). If the signal

MID(underscore)ACCEPT is HIGH, the latches LO1-LO3 will, therefore, be enabled when the clock signal PH1 is high whenever valid input data is loaded at the input of the stage, or when the latched data is a duplicate.

From...

...on the downstream latch LVOUT, with the reset signal being propagated backwards to cause the upstream validation latch to be forced low on the next clock cycle.

It should be noted that in the example shown in Fig. 8, the duplication of data contained in DATA tokens serves only as an...

...timing diagram for the data duplication circuit shown in Figs. 8a and 8b. As before, the timing diagram shows the relationship between the two-phase clock signals, the various internal and external control signals, and the manner in which data is clocked between the input and output sides of the stage and is duplicated.

Referring now more particularly to Figure 10, there is shown a reconfigurable process...This ordering of transmitted frames requires only two frames to be kept in memory at any one time, and does not require the decoder to wait for the transmission of the next P frame or I frame to display an interjacent B frame.

Further information will become more readily apparent to...

...In a first embodiment, in accordance with the present invention, as previously described with reference to Figures 10-12 an address generator is employed to store a block of formatted data, output from either the first decoder (Spatial Decoder) or the combination of the first decoder (Spatial Decoder) and the second...world, e.g. PAL-NTSC television standards. This is accomplished by selectively dropping or repeating pictures in a manner which is unique. Ordinary "frame rate converters," e.g. 2-3 pulldown, operate with a fixed input picture rate, whereas the Video Formatter can handle a variable input picture rate.

6. RECONFIGURABLE PROCESSING STAGE

Referring...RPS, it is decoded in the token decode circuit 33 and appropriate action will be taken. If it is not recognized, it will be passed unchanged to the output two-wire interface 42 through the output circuit 41. The present invention operates as a pipeline processor having a two-wire interface...interface to ensure that no further processing takes place using these 3 bytes. The decode register is emptied, and the value decode shift register 230 waits for the value to be shifted all the way over to such register.

The contents now of the low order bit positions of the value...

...serial pipeline processor for handling. The technique used is to study all the parameters of the multi-standards that are selected for processing by the serial processor and noting 1) their similarities, 2) their dissimilarities, 3) their needs and requirements and 4) selecting the correct token function to effectively process all of the standard signals sent into the...DRAM and its own DRAM interface.

Furthermore, while the DRAM interface is compression standard-independent, it still must be configured to implement each of the multiple standards, H.261, JPEG and MPEG. How the DRAM interface is reconfigured for multi-standard operation will be subsequently further described herein.

Accordingly, to understand...construction of both the address generator and the DRAM interface, as discussed further below.

In the present invention, the DRAM interface can operate from a

clock which is asynchronous to both the address generator and to the clocks of the stages through which data is passed. Special techniques have been used to handle this asynchronous nature of the operation.

Data is typically transferred...

...an address, it waits for the address generator to supply a valid address, processes that address and then sets the accept line high for one clock period. Thus, it implements a request/acknowledge (REQ/ACK) protocol.

A unique feature of the DRAM interface 302 is its ability to communicate independently with into RAM1. Data continues to be written into RAM1 311 until either there is no more data, or RAM1 is full. When RAM1 311 is full, the input side gives up control and sends a signal to the read side to indicate that RAM1 is now ready to be read. This signal passes between two asynchronous clock regimes and, therefore, passes through three synchronizing flip flops.

Provided RAM2 312 is empty, the next item of data to arrive on the input side...block in the present invention uses timing chains to place the edges of the DRAM signals to a precision of a quarter of the system clock period. Two quadrature clocks from the phase locked loop are used. These are combined to form a notional 2x clock. Any one chain is then made from two shift registers in parallel, on opposite phases of the 2x clock.

First of all, there is one chain for the page start cycle and another for the read/write/refresh cycles. The length of each cycle...is created. The pulse travels along the chains and is directed by the state information from the DRAM interface. The pulse generates the DRAM interface clock. Each DRAM interface clock period corresponds to one cycle of the DRAM, consequently, as the DRAM cycles have different lengths, the DRAM interface clock is not at a constant rate.

Moreover, additional timing chains combine the pulse from the above chains with the information from the DRAM interface to...

...interface (MPI) is used on all circuits with in the Spatial Decoder and Temporal Decoder. The MPI operates asynchronously with various Spatial and Temporal Decoder clocks. Referring to Table A.6.1 of the subsequent further detailed description, there is shown the various MPI signals that are used on this interface...between the Inverse modeller and inverse DCT (IDCT).

For example, in the present invention, an adder in the Inverse Quantizer is used to add a constant to the pel decode number before the data moves on to the IDCT.

The IDCT uses the pel decode number, which will vary according to... forth in the following sections.

(center dot) Description of features common to chips in the chip-set:
(Tokens
(Two wire interfaces
(DRAM interface
(Microprocessor interface
(Clocks
(Description of the Spatial Decoder chip
(Description of the Temporal Decoder chip

SECTION A.1

The first description section covers the majority of the electrical...
...2:0
(Flexible chroma sampling formats
(Full JPEG baseline decoding
(Glue-less page mode DRAM interface

(208 pin PQFP package
(Independent coded data and decoder clocks
(Re-orders MPEG picture sequence

The Video decoder family provides a low chip count solution for implementing high resolution digital video decoders. The chip-set...to control the flow of information. Data is only transferred between blocks when both the sender and receiver are observed to be ready when the clock rises.

1)Data transfer
2)Receiver not ready
3)Sender not ready

If the sender is not ready (as in 3 Sender not ready above...

...PCB tracks between chips. Where possible, track lengths should be kept below 25 mm. The PCB track capacitance should be kept to a minimum.

The clock distribution should be designed to minimize the clock slew between chips. If there is any clock slew, it should be arranged so that "receiving chips" see the clock before "sending chips".1)

All chips communicating via two wire interfaces should operate from the same digital power supply.

A.4.5 Interface timing

1...

...shows the two-wire interface between the system de-mux chip and the coded data port of the Spatial Decoder operating from the main decoder clock. This is optional as this two wire interface can work from the coded data clock which can be asynchronous to the decoder clock. See Section A.10.5, "Coded data clock". Similarly the display interface of the Image Formatter can operate from a clock that is asynchronous to the main decoder clock.

A.4.6 - Signal levels

The two-wire interface uses CMOS inputs and output. V1Hmm)) is approx. 70% of VDD)) and VH.max)) is approx...

...Table A.4.3 are those for V1H)) and V1L)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V.

A.4.7 Control clock

In general, the clock controlling the transfers across the two wire interface is the chip's decoder(underscore)clock. The exception is the coded data port input to the Spatial Decoder. This is controlled by coded(underscore)clock. The clock signals are further described herein.

SECTION A.5 DRAM Interface

A.5.1 The DRAM interface

A single high performance, configurable, DRAM interface is used... registers of the present invention can be read at any time.

A.5.4 Interface timing (ticks)

The-DRAM interface timing is derived from a Clock which is running at four times the input Clock rate of the device (decoder(underscore)clock). This clock is generated by an on-chip PLL.

For brevity, periods of this high speed clock are referred to as ticks.

A.5.5 Interface registers

A.5.6 Interface operation

The DRAM interface uses fast page mode. Three different types... determined by the register, refresh(underscore)interval.

The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 decoder(underscore)**clock** cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface to continuously...

...ordinary skill in the art will appreciate that microprocessor interfaces of other widths may also be used. The MPI operates synchronously to various decoder chip **clocks**.

A.6.1 MPI signals

...have no application in the normal use of the devices and need not be accessed by normal device configuration and control software.

SECTION A.7 **Clocks**

In accordance with the present inventions, many different **clocks** can be identified in the video decoder system. Examples of **clocks** are illustrated in Figure 56.

As data passes betweene different **clock** regimes within the video decoder chip-set, it is resynchronized (on-ship) to each new **clock**. In the present invention, the maximum frequency of any input **clock** is 30 MH2)). However, one of ordinary skill in the art will appreciate that other frequencies, including those greater than 30MHz, may also be used. On each chip, the microprocessor interface (MPI) operates asynchronously to the chip **clocks**. In addition, the Image Formatter can generate a low frequency audio **clock** which is synchronous to the decoded video's picture rate. Accordingly, this **clock** can be used to provide audio/video synchronization.

A.7.1 Spatial Decoder **clock** signals

The Spatial Decoder has two different (and potentially asynchronous) **clock** inputs:

A.7.2 Temporal Decoder **clock** signals

The Temporal Decoder has only one **clock** input:

A.7.3 Electrical specifications

A.7.3.1 CMOS levels

The **clock** input signals are CMOS inputs. VlHmin)) is approx. 70% of VDD)) and VILmax)) is approx. 30% of VDD)). The values shown in Table A.7.4 are those for VIH)) and VIL)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V.

A.7.3.2 Stability of **clocks**

In the present invention, **clocks** used to drive the DRAM interface and the chip-to-chip interfaces are derived from the input **clock** signals. The timing specifications for these interfaces assume that the input **clock** timing is stable to within (+-) 100 ps.

SECTION A.8 JTAG

As circuit boards become more densely populated, it is increasingly difficult to verify the...

...pins. The trst (Test Reset) pin resets the JTAG circuitry, to ensure

that the device doesn't power-up in test mode. The tck (Test Clock) pin is used to clock serial test patterns into the tdi (Test Data Input) pin, and out of the tdo (Test Data Output) pin. Lastly, the operational mode of the JTAG circuitry is set by clocking the appropriate sequence of bits into the tms (Test Mode Select) pin.

The JTAG standard is extensible to provide for additional features at the discretion...

...Full JPEG baseline decoding
(Glue-less DRAM interface
(Single +5V supply
(208 pin PQFP package
(Max. power dissipation 2.5W
(Independent coded data and decoder clocks
(Uses standard page mode DRAM

The Spatial Decoder is a configurable VLSI decoder chip for use in a variety of JPEG, MPEG and H.261...sampled at the same time as data (7:0), coded(underscore)extn and coded(underscore)valid, i.e., on the rising edge of coded(underscore)clock.

A.10.1.2 Byte mode

If, however, byte(underscore)mode is high, then a byte of data is transferred on data(7:0) under...A.11). The Start code Detector analyses data in the DATA Tokens bit serially. The Detector's normal rate of processing is one bit per clock cycle (of coded(underscore) clock). Accordingly, it will typically decode a byte of coded data every 8 cycles of coded(underscore)clock. However, extra processing cycles are occasionally required, e.g., when a non-DATA Token is supplied or when a start code is encountered in the...

...buffer newly arriving coded data (or stop new data for arriving) if the Spatial decoder is unable to accept data.

A.10.5 Coded data clock

In accordance with the present invention, the coded data port, the input circuit and other functions in the Spatial Decoder are controlled by coded(underscore)clock. Furthermore, this clock can be asynchronous to the main decoder(underscore)clock. Data transfer is synchronized to decoder(underscore)clock on-chip.

SECTION A.11 Start code detector

A.11.1 Start codes

As is well known in the art, MPEG and H.261 coded...of the buffers ensures that the buffers never empty during decoding and, this, therefore ensures that the decoder is able to decode new pictures at regular intervals.

Generally, two facilities are required to correctly start-up a decoder. First, there must be a mechanism to measure how much data has been provided...up delay for the first picture, the requirements of all subsequent pictures will be met automatically.

MPEG, therefore, specifies the start-up requirements as a delay. However, in a constant bit rate system this delay can readily be converted to a bit count. This is the basis on which the start-up control of the Spatial Decoder of the present...four main processing blocks in the Video Demux: Parser State Machine, Huffman decoder (including an ITOD), Macroblock counter and ALU.

The Parser or state machine follows the syntax of the coded video data and instructs the other units. The Huffman decoder converts variable length coded (VLC) data into integers. The Macroblock counter keeps track of which section of a picture is being

decoded. The ALU performs the...from the coded data and used to configure the Spatial Decoder. In this case the user must service the parser error ERR(underscore)MPEG(underscore)**SEQUENCE**, see A.14.8, "**Changes** at the MPEG **sequence** layer".

A.14.4.5 JPEG

Within baseline JPEG, there are a number of encoder options that significantly alter the complexity of the control software... underscore)information(underscore)picture. If there is only a single byte of extra(underscore)information(underscore)picture, no Parser event will occur.

A.14.8 **Changes** at the MPEG **sequence** layer

The MPEG **sequence** header describes the **following** characteristic of the video about to be decoded:

(horizontal and vertical size
(pixel aspect ratio
(picture rate
(coded data rate
(video buffer verifier buffer size...which of the Tokens are available at the output of the Spatial Decoder and which are most useful when designing circuits to display that output. **Other** Tokens will be present, but are not needed to display the output and, therefore, are not discussed here.

This section concentrates on showing:

(How the...

...operation

(Provides temporal decoding for MPEG & H.261 video decoders
(H.261 CIF and QCIF formats
(MPEG video resolutions up to 704x480, 30 Hz, 4:2:0
(Flexible chroma sampling formats
(Can re-order the MPEG picture **sequence**
(Glue-less DRAM interface
(Single +5V supply
(208 pin PQFP package
(Max. power dissipation 2.5W
(Uses standard page mode DRAM

The Temporal Decoder is a companion chip to the Spatial Decoder. It provides the temporal decoding required by H...

37/3,K/13 (Item 13 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00711604
Serial data processing using a pipeline

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FULLTEXT AVAILABILITY:
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CLAIMS B (English) 200107 1004
CLAIMS B (German) 200107 995
CLAIMS B (French) 200107 1110
SPEC B (English) 200107 121334
Total word count - document A 0
Total word count - document B 124443
Total word count - documents A + B 124443

...SPECIFICATION 2) illustrate the control of data transfer between stages of a preferred embodiment of a pipeline using a two-wire interface and a multi-phase **clock**;
Figure. 4 is a block diagram that illustrates a basic embodiment of a pipeline stage that incorporates a two-wire transfer control and also shows...

...in an exemplifying "data duplication" pipeline stage;
Figures. 9a and 9b taken together depict one example of a timing diagram that shows the two-phase **clock**, the two-wire transfer control signals and the other internal data and control signals used in the exemplifying embodiment shown in Figures. 8a and 8b...

...shows a macroblock structure;
Figure 37 shows a two-wire interface protocol;
Figure 38 shows the location of external two-wire interfaces;
Figure 39 shows **clock** propagation;
Figure 40 shows two-wire interface timing;
Figure 41 shows examples of access structure;
Figure 42 shows a read transfer cycle;
Figure 43 shows...

...timing;
Figure 54 shows an MPI write timing;
Figure 55 shows organization of large integers in the memory map;
Figure 56 shows a typical decoder **clock** regime;
Figure 57 shows input **clock** requirements;
Figure 58 shows the Spatial Decoder;
Figure 59 shows the inputs and outputs of the input circuit;
Figure 60 shows the coded port protocol;
Figure 61 shows the start code detector;
Figure 62 shows start codes detected and **converted** to Tokens;
Figure 63 shows the start codes detector passing Tokens;
Figure 64 shows overlapping MPEG start codes (byte aligned);
Figure 65 shows overlapping MPEG...of blocks;
Figure 95 shows an H.261 "slice" layer;
Figure 96 shows an H.261 arrangement of macroblocks;
Figure 97 shows an H.261 **sequence** of blocks;

Figure 98 shows an H.261 macroblock layer;

Figure 99 shows an H.261 arrangement of pels in blocks;

Figure 100 shows a...of pipeline stages. Furthermore, data may be processed in more than one stage and the processing time for different stages can differ.

In addition to clock and data signals (described below), the pipeline includes two transfer control signals -- a "VALID" signal and an "ACCEPT" signal. These signals are used to control...3) illustrate generally a preferred embodiment of the pipeline. This preferred embodiment implements the structure shown in Fig. 2 using a two-phase, non-overlapping clock with phases (o slash)0 and (o slash)1. Although a two-phase clock is preferred, it will be appreciated that it is also possible to drive the various embodiments of the invention using a clock with more than two phases.

As shown in Fig. 3, each pipeline stage is represented as having two separate boxes which illustrate the primary and...

...the various pipeline stages as before, for ease of illustration, only the ACCEPT signal is shown in Fig. 3. A change of state during a clock phase of certain of the ACCEPT signals is indicated in Fig. 3 using an upward-pointing arrow for changes from LOW to HIGH. Similarly, a ...

...HIGH whenever the storage elements contain valid data.

In Fig. 3, each cycle is shown as consisting of a full period of the non-overlapping clock phases (o slash)0 and (o slash)1. As is explained in greater detail below, data is transferred from the secondary storage elements (shown as the left box in each stage) to the primary storage elements (shown as the right box in each stage) during clock cycle (o slash)1, whereas data is transferred from the primary storage elements of one stage to the secondary storage elements of the following stage during the clock cycle (o slash)0. Fig. 3 also illustrates that the primary and secondary storage elements in each stage are further connected via an internal acceptance...ACCEPT signal into Stage F remains LOW, data upstream of Stage F can continue to be shifted between stages and within stages on the respective clock phases until the next valid data block D3 reaches the primary storage elements of Stage E. As illustrated, this condition is reached during the (o...

...data, and it signals this by setting the ACCEPT signal into Stage E LOW.

When the ACCEPT signal into the pipeline from the downstream device changes from LOW to HIGH or vice versa, this change does not have to propagate upstream within the pipeline further than to the immediately preceding storage elements (within the same stage or within the preceding pipeline stage). Rather, this change propagates upstream within the pipeline one storage element block per clock phase.

As this example illustrates, the concept of a "stage" in the pipeline structure illustrated in Fig. 3 is to some extent a matter of...signal LOW not only when all of the downstream storage elements are filled with valid data, but also when a stage requires more than one clock phase to finish processing its data. This also can occur when it creates valid data in one or both of its storage elements. In other...

...process analog signals.

As discussed previously, while other conventional timing arrangements may be used, the interface is preferably controlled by a two-phase, non-overlapping clock. In Figs. 4-9, these clock phase signals are referred to as PH0 and PH1. In Fig. 4, a line is shown for each clock phase signal.

Input data enters a pipeline stage over a multi-bit data bus

IN(underscore)DATA and is transferred to a following pipeline stage...

...example of this embodiment, it is assumed that the Q outputs of all latches follow their D inputs, that is, they are "loaded", when the clock input is HIGH, i.e., at a logic "1" level. Additionally, the Q outputs hold their last values. In other words, the Q outputs are "latched" on the falling edge of their respective clock signals. Each latch has for its clock either one of two non-overlapping clock signals PH0 or PH1 (as shown in Fig. 5), or the logical AND combination of one of these clock signals PH0, PH1 and one logic signal. The invention works equally well, however, by providing latches that latch on the rising edges of the clock signals, or any other known latching arrangement, as long as conventional methods are applied to ensure proper timing of the latching operations.

The output data...the Q signal and/or its logical inverse.

The data and validation latches LDIN, LDOUT, LVIN and LVOUT, load their respective data inputs when both clock signals (PH0 at the input side and PH1 at the output side) and the output from the acceptance latch of the same side are logical "1". Thus, the clock signal (PH0 for the input latches LDIN and LVIN) and the output of the respective acceptance latch (in this case, LAIN) are used in a...

...and QAIN are both "1". It will latch this data when either of these two signals goes to a "0".

Although only one of the clock phase signals PH0 or PH1, is used to clock the data and validation latches at the input (and output) side of the pipeline stage, the other clock phase signal is used, directly, to clock the acceptance latch at the same side. In other words, the acceptance latch on either side (input or output) of a pipeline stage is preferably clocked "out of phase" with the data and validation latches on the same side. For example, PH1 is used to clock the acceptance input latch, although PH0 is used in generating the clock signal CK for the data latch LDIN and the validation latch LVIN.

As an example of the operation of a pipeline augmented by the two...

...signal IN(underscore)VALID to the illustrated stage has not gone to a "1" since the system was most recently reset. Assume further that several clock cycles have taken place since the system was last reset and, accordingly, the circuitry has reached a steady-state condition. The validation input signal QVIN from the validation latch LVIN is, therefore, loaded as a "0" during the next positive period of the clock PH0. The input to the acceptance input latch LAIN (via the gate NAND1 or another equivalent gate, is, therefore, loaded as a "1" during the next positive period of the clock signal PH1. In other words, since the data in the data input latch LDIN is not valid, the stage signals that it is ready to...

...transparent latches so that whatever data is on the IN(underscore)DATA bus simply is loaded into the data latch LDIN as soon as the clock signal PHO goes to a "1". Of course, this invalid data will also be loaded into the next data latch LDOUT of the following pipeline...

...a data latch does not contain valid data, it accepts or "loads" any data presented to it during the next positive period of its respective clock signal. On the other hand, such invalid data is not loaded in any stage for which the acceptance signal from its corresponding acceptance latch is...

...by rising to a "1". The output of the corresponding validation latch then rises to a "1" on the next rising edge of its respective clock phase signal. For example, the validation input signal QVIN of latch LVIN

rises to a "1" when its corresponding IN(underscore)VALID signal goes high (that is, rises to a "1") on the next rising edge of the clock phase signal PH0.

Assure now, instead, that the data input latch LDIN contains valid data. If the data output latch LDOUT is ready to accept new data, its acceptance signal QAOUT will be a "1". In this case, during the next positive period of the clock signal PH1, the data latch LDOUT and validation latch LVOUT will be enabled, and the data latch LDOUT will load the data present at its input. This will occur before the next rising edge of the other clock signal PH0, since the clock signals are non-overlapping. At the next rising edge of PH0, the preceding data latch (LDIN) will, therefore, not latch in new input data from...

...latches (within a stage or between adjacent stages) that are able to accept data, since they will be operating based on alternate phases of the clock. Any data latch that is not ready to accept new data because it contains valid data that cannot yet be passed, will have an output...the state of the validation input signal QVIN. The acceptance input signal QAIN then rises to a "1" at the next rising edge of the clock signal PH1. Assuming that the validation signal IN(underscore)VALID has been correctly reset to a "0", then upon the subsequent rising edge of the clock signal PH0, the output from the validation latch LVIN will become a "0", as it would have done if it had been reset directly.

As...

...latch: If the reset signal NOTRESET0 can be guaranteed to be low during more than one complete cycle of both phases PH0, PH1 of the clock, then the "automatic reset" (a backwards propagation of the reset signal) will occur for validation latches in preceding pipeline stages. Indeed, if the reset signal is held low for at least as many full cycles of both phases of the clock as there are pipeline stages, it will only be necessary to directly reset the validation output latch in the final pipeline stage.

Figs. 5a and 5b (referred to collectively as Fig. 5) illustrate a timing diagram showing the relationship between the non-overlapping clock signals PH0, PH1, the effect of the reset signal, and the holding and transfer of data for the different permutations of validation and acceptance signals...the stage depends upon stored state information, which is another way of saying it must retain some information about its own history one or more clock cycles ago. The present invention is well-suited for use in pipelines that include such "state machine" stages, as well as for use in applications...

...The value of the extension bit is loaded into LEIN and is then loaded into LEOUT on the next rising edge of the non-overlapping clock phase signal PH1. Latch LEOUT, thus, contains the value of the current extension bit, but only during the second half of the non-overlapping, two-phase clock. Latch LEPREV, however, loads this extension bit value on the next rising edge of the clock signal PHO, that is, the same signal that enables the extension bit input latch LEIN. The output QEPREV of the latch LEPREV, thus, will hold the value of the extension bit during the previous PHO clock phase.

The five bits of the data word output from the inverting Q output, plus the non-inverted MD(2), of the latch LDIN are...of the extension bit at the input and at the output of the stage, respectively. As Fig. 8a shows, the input extension latch LEIN is clocked synchronously with the input data latch LDIN and the validation signal IN(underscore)VALID.

In the duplication stage, the output from the data latch LDIN...of the intermediate extension bit (labeled "MID(underscore)EXTN" and as signal

S4), and it loads this value on the next rising edge of the clock phase PHO into the latch LI1, whose output is the bit QI1 and is one of the inputs to the token decoding logic group that...

...both QI1 and S1 are HIGH, the signal DATA(underscore)TOKEN will retain its state (whether "0" or "1"). This is true even though the clock signals PHO and PH1 are clocking the latches (LI2 and LO2 respectively). The value of DATA(underscore)TOKEN can only change when one or both of the signals QI1 and S1...

...S2 will thus be a "0". As a result, this "0" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "0", indicating that the circuitry is not processing a DATA token.

If QI1 is "0" and...

...NAND22 from the output of NAND20). As a result, this "1" value will be loaded into latch LO2 at the start of the next PH1 clock phase and the DATA(underscore)TOKEN signal will become "1", indicating that the circuitry is processing a DATA token.

The NOT(underscore)DUPLICATE signal (the output signal QO3) is similarly loaded into the latch LI3 on the next rising edge of the clock PHO. The output signal QI3 from the latch LI3 is combined with the output signal QI2 in a gate NAND24 to form the signal S3...

...is not a duplicate (QI3 = 0), then the signal S3 goes high.

Assume now, that the DATA TOKEN signal remains HIGH for more than one clock signal. Since the NOT(underscore)DUPLICATE signal (QO3) is "fed back" to the latch LI3 and will be inverted ...states, so that the input latches will be enabled and will be able to accept data, at most, during every other complete cycle of both clock phases PH0, PH1. The additional condition that the following stage be prepared to accept data, as indicated by a "HIGH" OUT(underscore)ACCEPT signal, must...

...be satisfied. The output latch LDOUT will, therefore, place the same data word onto the output bus OUT(underscore)DATA for at least two full clock cycles. The OUT(underscore)VALID signal will be a "1" only when there is both a valid DATA(underscore)TOKEN (QO2 HIGH) and the validation...

...is a duplicate (QI3 is a "O"). If the signal MID(underscore)ACCEPT is HIGH, the latches LO1-LO3 will, therefore, be enabled when the clock signal PH1 is high whenever valid input data is loaded at the input of the stage, or when the latched data is a duplicate.

From...on the downstream latch LVOUT, with the reset signal being propagated backwards to cause the upstream validation latch to be forced low on the next clock cycle.

It should be noted that in the example shown in Fig. 8, the duplication of data contained in DATA tokens serves only as an...

...timing diagram for the data duplication circuit shown in Figs. 8a and 8b. As before, the timing diagram shows the relationship between the two-phase clock signals, the various internal and external control signals, and the manner in which data is clocked between the input and output sides of the stage and is duplicated.

Referring now more particularly to Figure 10, there is shown a reconfigurable process...QUANT(underscore)TABLE) which goes down the processing pipeline. As far as that machine is concerned, all of that was data; it was handling data, transforming one sort of data into another sort of data, which is clearly a function of the processing performed by that portion of the machine. However, when that information gets to the...is capable of taking MPEG, JPEG and H.261 bit streams and

generating from them a sequence of proprietary tokens which are meaningful to the rest of the decoder. As an example of how multi-standard decoding is achieved, the MPEG (1 and 2) picture(underscore)start(underscore)code, the H of the standard signals indicated in Table 600. The Start Code Detector creates sequence (underscore)start, group(underscore)start, sequence(underscore)end, slice(underscore)start, user-data, extra-data and PICTURE(underscore)START tokens for application to the two-wire interface which is used throughout...which do not use control tokens.

The control tokens are generated by circuitry within the decoder processor and emulate the operation of a number of different type standard-dependent signals passing into the serial pipeline processor for handling. The technique used is to study all the parameters of the multi-standards that are selected for processing by the serial... construction of both the address generator and the DRAM interface, as discussed further below.

In the present invention, the DRAM interface can operate from a clock which is asynchronous to both the address generator and to the clocks of the stages through which data is passed. Special techniques have been used to handle this asynchronous nature of the operation.

Data is typically transferred...an address, it waits for the address generator to supply a valid address, processes that address and then sets the accept line high for one clock period. Thus, it implements a request/acknowledge (REQ/ACK) protocol.

A unique feature of the DRAM interface 302 is its ability to communicate independently with...

...control and sends a signal to the read side to indicate that RAM1 is now ready to be read. This signal passes between two asynchronous clock regimes and, therefore, passes through three synchronizing flip flops.

Provided RAM2 312 is empty, the next item of data to arrive on the input side...block in the present invention uses timing chains to place the edges of the DRAM signals to a precision of a quarter of the system clock period. Two quadrature clocks from the phase locked loop are used. These are combined to form a notional 2x clock. Any one chain is then made from two shift registers in parallel, on opposite phases of the 2x clock.

First of all, there is one chain for the page start cycle and another for the read/write/refresh cycles. The length of each cycle...

...is created. The pulse travels along the chains and is directed by the state information from the DRAM interface. The pulse generates the DRAM interface clock. Each DRAM interface clock period corresponds to one cycle of the DRAM, consequently, as the DRAM cycles have different lengths, the DRAM interface clock is not at a constant rate.

Moreover, additional timing chains combine the pulse from the above chains with the information from the DRAM interface to...interface (MPI) is used on all circuits with in the Spatial Decoder and Temporal Decoder. The MPI operates asynchronously with various Spatial and Temporal Decoder clocks. Referring to Table A.6.1 of the subsequent further detailed description, there is shown the various MPI signals that are used on this interface...of the Spatial Decoder. Note that at this point, there are as many tokens as will be used by the system.

26. INVERSE DISCRETE COSINE TRANSFORM

The Inverse Discrete Cosine Transform (IDCT), in accordance with the present invention, decompresses data related to the frequency of the DC component of the picture. When a particular picture is...is set forth in the following sections.

. Description of features common to chips in the chip-set:

. Tokens
. Two wire interfaces
. DRAM interface
. Microprocessor interface
. **Clocks**
. Description of the Spatial Decoder chip
. Description of the Temporal Decoder chip

SECTION A.1

The first description section covers the majority of the electrical...

...2:0

(Flexible chroma sampling formats
(Full JPEG baseline decoding
(Glue-less page mode DRAM interface
(208 pin PQFP package
(Independent coded data and decoder **clocks**
(Re-orders MPEG picture sequence

The Video decoder family provides a low chip count solution for implementing high resolution digital video decoders. The chip-set...to control the flow of information. Data is only transferred between blocks when both the sender and receiver are observed to be ready when the **clock** rises.

1)Data transfer
2)Receiver not ready
3)Sender not ready If the sender is not ready (as in 3 Sender not ready above...

...the interface concerned (See Figure 35, "Tokens on interfaces wider than 8 bits". For example, 12 bit coefficients are input to the Inverse Discrete Cosine **Transform** (IDCT), but only 9 bits are output.

In addition to the data signals there are three other signals transmitted via the two-wire interface:

. valid...

...PCB tracks between chips. Where possible, track lengths should be kept below 25 mm. The PCB track capacitance should be kept to a minimum.

The **clock** distribution should be designed to minimize the **clock** slew between chips. If there is any **clock** slew, it should be arranged so that "receiving chips" see the **clock** before "sending chips".1)1) Note: Figure 38 shows the two-wire interface between the system de-mux chip and the coded data port of the Spatial Decoder operating from the main decoder **clock**. This is optional as this two wire interface can work from the coded data **clock** which can be asynchronous to the decoder **clock**. See Section A.10.5, "Coded data **clock**". Similarly the display interface of the Image Formatter can operate from a **clock** that is asynchronous to the main decoder **clock**.)

All chips communicating via two wire interfaces should operate from the same digital power supply.

A.4.5 Interface timing

A.4.6 - Signal levels...

...Table A.4.3 are those for V1H)) and V1L)) at their respective worst case VDD)). VDD))=5.0(+-)0.25V .

A.4.7 Control **clock**

In general, the **clock** controlling the transfers across the two wire interface is the chip's decoder(underscore)**clock**. The

exception is the coded data port input to the Spatial Decoder. This is controlled by coded(underscore)**clock**. The **clock** signals are further described herein.

SECTION A.5 DRAM Interface

A.5.1 The DRAM interface

A single high performance, configurable, DRAM interface is used... registers of the present invention can be read at any time.

A.5.4 Interface timing (ticks)

The DRAM interface timing is derived from a **Clock** which is running at four times the input **Clock** rate of the device (decoder(underscore)**clock**). This **clock** is generated by an on-chip PLL.

For brevity, periods of this high speed **clock** are referred to as ticks.

A.5.5 Interface registers

A.5.6 Interface operation

The DRAM interface uses fast page mode. Three different types... determined by the register, refresh(underscore)interval.

The value in refresh(underscore)interval specifies the interval between refresh cycles in periods of 16 decoder(underscore)**clock** cycles. Values in the range 1.255 can be configured. The value 0 is automatically loaded after reset and forces the DRAM interface to continuously...

...ordinary skill in the art will appreciate that microprocessor interfaces of other widths may also be used. The MPI operates synchronously to various decoder chip **clocks**.

A.6.1 MPI signals

A.6.2 - MRI electrical specifications
A.6.2.1 AC characteristics

A.6.3 Interrupts

In accordance with the...have no application in the normal use of the devices and need not be accessed by normal device configuration and control software.

SECTION A.7 **Clocks**

In accordance with the present inventions, many different **clocks** can be identified in the video decoder system. Examples of **clocks** are illustrated in Figure 56.

As data passes between different **clock** regimes within the video decoder chip-set, it is resynchronized (on-chip) to each new **clock**. In the present invention, the maximum frequency of any input **clock** is 30 MHz)). However, one of ordinary skill in the art will appreciate that other frequencies, including those greater than 30MHz, may also be used. On each chip, the microprocessor interface (MPI) operates asynchronously to the chip **clocks**. In addition, the Image Formatter can generate a low frequency audio **clock** which is synchronous to the decoded video's picture rate. Accordingly, this **clock** can be used to provide audio/video synchronization.

A.7.1 Spatial Decoder **clock** signals

The Spatial Decoder has two different (and potentially asynchronous) clock inputs:

A.7.2 Temporal Decoder clock signals

The Temporal Decoder has only one clock input:

A.7.3 Electrical specifications

A.7.3.1 CMOS levels

The clock input signals are CMOS inputs. VIHmin)) is approx. 70% of VDD)) and VILmax)) is approx. 30% of VDD)). The values shown in Table A.7.4 are those for VIH)) and VIL)) at their respective worst case VDD)). vDD)) = 5.0(+-)0.25V.

A.7.3.2 Stability of clocks

In the present invention, clocks used to drive the DRAM interface and the chip-to-chip interfaces are derived from the input clock signals. The timing specifications for these interfaces assume that the input clock timing is stable to within (+-) 100 ps.

SECTION A.8 JTAG

As circuit boards become more densely populated, it is increasingly difficult to verify the...

...pins. The trst (Test Reset) pin resets the JTAG circuitry, to ensure that the device doesn't power-up in test mode. The tck (Test clock) pin is used to clock serial test patterns into the tdi (Test Data Input) pin, and out of the tdo (Test Data Output) pin. Lastly, the operational mode of the JTAG circuitry is set by clocking the appropriate sequence of bits into the tms (Test Mode Select) pin.

The JTAG standard is extensible to provide for additional features at the discretion...

...Full JPEG baseline decoding
. Glue-less DRAM interface
. Single +5V supply
. 208 pin PQFP package
. Max. power dissipation 2.5W
. Independent coded data and decoder clocks
. Uses standard page mode DRAM

The Spatial Decoder is a configurable VLSI decoder chip for use in a variety of JPEG, MPEG and H.261...

...r(underscore)buffer(underscore)size 0x157:0 0x167:4not used 3:0pel(underscore)aspect r(underscore)pel(underscore)aspect 0x177:2not used 1:0bit(underscore)rate r(underscore)bit(underscore)rate 0x187:0 0x197:0 0x1A7:4not used 3:0pic(underscore)rate r(underscore)pic(underscore)rate 0x1B7:1not used 0constrained r(underscore)constrained 0x1C7:0picture underscore)frame(underscore)change 0x237:0private register MEPG full(underscore)pel(underscore)bwd, JPEG restart index 0x247:0private register horiz(underscore)mb(underscore)copy 0x257:0pic(underscore)number 0x267:1not used 1:0max(underscore)h 0x277:1not used 1:0max(underscore)v 0x287:0private register scratch1 0x297:0private register...

...underscore)name(underscore)0 r(underscore)c(underscore)0 0x3D7:0component(underscore)name(underscore)1 r(underscore)c(underscore)1 0x3E7:0component(underscore)name(underscore)2 r(underscore)c(underscore)2 0x3F7:0component(underscore)name(underscore)3

r(underscore)c(underscore)3 0x407:0private registers 0x63 0x407:0r(underscore)dc(underscore...sampled at the same time as data (7:0), coded(underscore)extn and coded(underscore)valid, i.e., on the rising edge of coded(underscore)**clock**.

A.10.1.2 Byte mode

If, however, byte(underscore)mode is high, then a byte of data is transferred on data (7:0) under...

...the interface is ready to accept more data.

A.10.3 Switching between input modes

Provided suitable precautions are observed, it is possible to dynamically **change** the data input mode. In general, the transfer of a Token via any one route should be completed before **switching** modes.

The first byte supplied in byte mode causes a DATA Token header to be generated on-chip. Any further bytes transferred in byte mode...

...A.11). The Start code Detector analyses data in the DATA Tokens bit serially. The Detector's normal rate of processing is one bit per **clock** cycle (of coded(underscore)**clock**). Accordingly, it will typically decode a byte of coded data every 8 cycles of coded(underscore)**clock**. However, extra processing cycles are occasionally required, e.g., when a non-DATA Token is supplied or when a start code is encountered in the...

...buffer newly arriving coded data (or stop new data for arriving) if the Spatial decoder is unable to accept data.

A.10.5 Coded data **clock**

In accordance with the present invention, the coded data port, the input circuit and other functions in the Spatial Decoder are controlled by coded(underscore)**clock**. Furthermore, this **clock** can be asynchronous to the main decoder(underscore)**clock**. Data transfer is synchronized to decoder(underscore)**clock** on-chip.

SECTION A.11 Start code detector

A.11.1 Start codes

As is well known in the art, MPEG and H.261 coded...Token when it detects information that indicates that the current picture has been completed.

The Tokens that cause PICTURE(underscore)END to be generated are: **SEQUENCE**(underscore)START, GROUP(underscore)START, PICTURE(underscore)START, **SEQUENCE**(underscore)END and FLUSH.

A.11.7.**2** Stop after picture end option

If the register stop(underscore)after(underscore)picture is set, then the Start Code Detector will stop after a PICTURE...

...of the buffers ensures that the buffers never empty during decoding and, this, therefore ensures that the decoder is able to decode new pictures at **regular intervals**.

Generally, two facilities are required to correctly start-up a decoder. First, there must be a mechanism to measure how much data has been provided...up delay for the first picture, the requirements of all subsequent pictures will be met automatically.

MPEG, therefore, specifies the start-up requirements as a **delay**. However, in a **constant** bit rate system this **delay** can readily be converted to a bit count. This is the basis on which the start-up control of the Spatial Decoder of the present...four main processing

blocks in the Video Demux: Parser State Machine, Huffman decoder (including an ITOD), Macroblock counter and ALU.

The Parser or state machine follows the syntax of the coded video data and instructs the other units. The Huffman decoder converts variable length coded (VLC) data into integers. The Macroblock counter keeps track of which section of a picture is being decoded. The ALU performs the...from the coded data and used to configure the Spatial Decoder. In this case the user must service the parser error ERR(underscore)MPEG(underscore)SEQUENCE, see A.14.8, "Changes at the MPEG sequence layer".

A.14. ...underscore)information(underscore)picture. If there is only a single byte of extra(underscore)information(underscore)picture, no Parser event will occur.

A.14.8 Changes at the MPEG sequence layer

The MPEG sequence header describes the following characteristic of the video about to be decoded:

(horizontal and vertical size
(pixel aspect ratio
(picture rate
(coded data rate
(video buffer verifier buffer size

If any of these parameters change when the Spatial Decoder decodes a sequence header, the Parser event ERR(underscore)MPEG(underscore)SEQUENCE will be generated.

A.14.8.1 Change in picture size

If the picture size has changed, the user's software should read the values...

37/3,K/15 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00566667 **Image available**
ADVANCED DEFERRED SHADING GRAPHICS PIPELINE PROCESSOR
PROCESSEUR PIPELINE GRAPHIQUE EVOLUE A OMBRAGE DIFFERE
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GO Shun Wai, 370 Sandhurst Drive, Milpitas, CA 95035, US,
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Patent and Priority Information (Country, Number, Date):
Patent: WO 200030040 A1 **20000525** (WO 0030040)
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Priority Application: US 9897336 19980820; US 98213990 19981217
Designated States:
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Patent and Priority Information (Country, Number, Date):
Patent: ...**20000525**
Fulltext Availability:
Detailed Description
Publication Year: **2000**

Detailed Description

... No. filed 20 August 1999, entitled SYSTEM, APPARATUS AND METHOD FOR BALANCING RENDERING RESOURCES IN A THREE-DIMENSIONAL GRAPHICS PIPELINE (Atty. Doc. No. A-66379);
Serial No. .., filed 20 August 1999, entitled GRAPHICS PROCESSOR WITH
PIPELINE STATE STORAGE AND RETRIEVAL (Atty. Doc. No. A-66378);
Serial No. .., filed 20 August 1999...

...this document, raster lines are generally numbered from bottom to top, but are displayed in order from top to bottom.

In a 3D animation, a **sequence** of images is displayed, giving the illusion of motion in three-dimensional space. Interactive 3D computer graphics allows a user to **change** his viewpoint or **change** the geometry in real-time, thereby requiring the rendering system to create new images on-the-fly in real-time.

In 3D computer graphics, each...system based on (Xeye1Yeye1Zeye) The object is projected onto the viewing plane, thereby correcting for perspective. At this point, the object appears to have become two-dimensional; however, the object's z-coordinates are

preserved so they can be used later by hidden surface removal techniques. The object is finally translated...only to objects that are closed volumes. The fourth step, lighting computation, generally includes the set up for Gouraud shading and/or texture mapping with multiple light sources of various types, but could also be set up for Phong shading or one of many other choices (Step 222). The fifth step...that the z-value be strictly "greater-than" for some objects and "greater-than-or-equal-to" for other objects. These particular depth tests which change from time to time, may be considered to be pipeline state at that time. Parameters considered to be renderer (pipeline) state in OpenGL are identified in Section 6.2 of the afore referenced OpenGL Specification (Version 1.2, at pages 193-217).

Essentially then, there are two types of data or information used by the renderer.

(1) primitive data which may be thought of as per-vertex data, and (ii) pipeline state the several tests that are typically performed sequentially beginning with a fragment and its associated data and finishing with the final output stream to the frame buffer are in the order performed (and...is a diagrammatic illustration showing a tetrahedron, with its own coordinate axes, a viewing point's coordinate system, and screen coordinates. [1 791 FIG. G 2 is a diagrammatic illustration showing a conventional generic renderer for a 3D graphics pipeline.[180]
FIG. G 3 is a diagrammatic illustration showing elements of...This picture generation is commonly referred to as rendering. The appearance of motion, for example in a 3-Dimensional animation is achieved by displaying a sequence of images.

Interactive -Dimensional (3D) computer graphics allows a user to change his or her viewpoint or to change the geometry in real-time, thereby requiring the rendering system to create new images - 26 on-the-fly in real-time. Therefore, real-time performance...pipeline state data.

In DSGPv2, the part of the pipeline state data needed for HSR is stored into spatial memory 261, while the rest is stored into polygon memory 262. Examples of pipeline state needed for HSR include (as defined, for example, in the OpenGL Specification) are DepthFunc, DepthMask, StencilEnable, etc. Examples of pipeline...SFSMs, labeled SFSMO through SFSM3) - 35 and an additional primitive (primitive B) covering two of those four samples. The three primitives are rendered in the following order (starting with a depth clear and with depth test set to less-than).

primitive A (with stencil test disabled); primitive B (with stencil test ...parallel, and generally all the samples in all the pixels within a stamp are done in parallel. Hence, if one stamp can be processed per clock cycle (and there are 4 pixels per stamp and 4 samples per pixel), then 16 samples are processed per clock cycle. A "stamp" defines the number of pixels and samples processed at one time. This per-stamp processing is generally pipelined, with pipeline stalls injected...Block. Mode Extraction Block inserts the appropriate color pointer in the Geometry packets.

Pipeline state is broken down into several categories to minimize storage as follows: (1) Spatial pipeline state includes data headed for Sort that changes every vertex; (2) Cull-mode state includes data headed for Cull (via Sort) that changes infrequently; (3) Color

includes data headed for Polygon memory that changes every vertex...

...address locations where the most recent changes to the respective state information is stored.

Each change in one of these state is identified by an **additional** entry at the end of a **sequentially** ordered state storage list stored in a memory. Effectively, all state changes are stored and when particular state corresponding to a point in time (or...desirable to make reuse of these textels, because if you're marching along in tile space, your pixel grid within the tile (typically processed along **sequential** rows in the rectangular tile pixel grid) could come such that while the same texture map is not needed for sequential pixels, the same texture...simple primitives like 1 5 triangles and quadrilaterals. However, as we shall see later, they can be obtained fairly easily, and they provide a nice **uniform** way to setup primitives.

Treating lines as rectangles (or equivalently interpreting rectangles as lines) involves specifying two end points in space and a width. Treating ...of the texture at a given magnification or minification. To produce a texture value for a given pixel fragment, TEX performs tri-linear interpolation (though **other** interpolation procedures may be used) from the texture maps, to approximate the correct level of detail for the viewing distance. TEX also performs other interpolation...

...VSPs) as well as cache fill packets that are passed through from MIJ. It is noted that in one embodiment, the cache fill packets are **stored** in RAM within PHG until needed. Fully interpolated stamps are forwarded by FRG to PHG (as well as to TEX and BUMP within ...Cache Fill packet (LtFill), Material Cache Fill packet (Will), and Begin Tile Packet (BegrinTile) from FRG over header and data busses. Recall also that MIJ **keeps** track of the contents of the Color, TexA, - 73 TexB, Light, and Material caches for PHG (as well as for FRG and TEX) and associates ...SMEM, TMEM, and FIRM are provided on seprate chips. An interchip communication ring is provided to couple the units on the chips for communication. In **other** embodiments of the invention, all functional blocks are provided on a single chip (common semiconductor substrate) 40 which may also include memory (PMEM, SMEM, TMEM...

...the units which consume them. CFD does some decoding and unpacking of commands, manages the AGP interface, and gets involved in DMA transfers and retains **some** state for context **switches**. It is one of the least glamorous, but most essential components of the DSGP system.

1 0 FIG. 18 shows a block diagram of the...block is - 88 capable of processing, in a pipelined manner, a hidden surface removal method on a stamp with the throughput of one stamp per **clock** cycle.

A primitive may touch many tiles and therefore, unlike traditional rendering pipelines, may be visited many times during the course of rendering the frame...packets to vary in length. The Color Pointer that is stored with every vertex indicates the location of the corresponding Color packet in Polygon Memory. **Some** shading data and operators **change** frequently, **others** less frequently, these may be saved in different structures or may be saved in one structure.

In one embodiment, in MEX, there is no default...In this embodiment, each of these nine tag caches are fully associative and use CAMs for cache tag lookup, allowing a lookup in a single **clock cycle**.

In one embodiment, these caches are listed in the table below.

Cache Block # entries
Color dualoct MIJ 32
MIm
ptr MIJ 32
ColorData FIRG 128...

...32
TextureB TEX 16
Material PHG 32
Light PHG 8
- 105
Cache Block entries
PixelMode PIX 1 6
Stipple PIX 4
In one embodiment, cache **replacement** policy is based on -the First In First Out (FIFO) logic for all caches in MIJ.

Color Caching in FIRG
"Color"caching is used to...or 4500.

Maximum per tile estimate element 1415 represents a value that corresponds to a "worst case," or maximum number of memory locations necessary to **store** the largest primitive that could occupy the 2-D **window**. This largest primitive would touch every tile in the 2-D window. Memory left element 1425 represents the actual amount of sort memory 315 that...

Patent Abstract Files

File 347:JAPIO Dec 1976-2006/Dec(Updated 070403)
File 350:Derwent WPIX 1963-2007/UD=200734

Set Items Description
S1 2173153 SAVE OR SAVING OR SAVED OR STORE OR STORED OR STORING OR K-EEP?
S2 708508 BACKUP? OR BACK??? () UP OR COPY OR COPIES OR COPYING OR -COPIED OR REBUILD? OR REPLACING OR REPLACEMENT? OR RESTORE? ? OR RESTORING OR RESTORED OR UPDATE OR UPDATING OR UPDATED
S3 95445 CLOCK (3N) (CYCLE? OR RATE?? ? OR SPEED? OR PULS??? OR CIR-CUIT?)
S4 424 S1 (50N) S2 (50N) S3
S5 345 TWO OR 2 OR MORE OR SOME OR MULTI OR MULTIPLE OR ANOTHER OR DIFFERENT OR OTHER? ? OR ADDITIONAL? OR BOTH OR MANY OR ASSO-RTED OR SEVERAL OR FEW OR SECOND OR DUPLICAT? OR DOUBL? OR DU-AL OR ITERAT? OR PLURAL OR TWIN? ? OR TWINNED
S6 193 CHANG??? OR CONVERT? OR EXCHANG? OR FLIP OR INTERCHANG??? -OR REPLAC??? OR SUBSTITUT??? OR SWAP??? OR SWITCH??? OR TRANS-FORM???
S7 3 TWICE
S8 345 S5 OR S7
S9 49 S6 (3N) S8
S10 49 S4 AND S9
S11 80 CHRONOLOGICAL? OR CONSECUTIVE? OR ENSUING OR FOLLOW???? OR-SEQUENCE?? ? OR SEQUENTIAL? OR SERIAL? OR SUCCED? OR SUCCESSI?
S12 12 S10 AND S11
S14 61 INTERVAL? ? OR LAG? ? OR LAGGING OR LAPSE? ? OR LATENC? OR LULL?? OR PAUSE? ? OR RECESS?? OR RESPITE OR REST? ? OR STAL-L??? OR STAY?? OR SUSPENSION? ? OR WAIT? ? OR WAITING
S15 106 ABEYANCE OR BREAK??? OR BREATHER OR DELAY? OR FREEZ? OR GA-P? ? OR HALT??? OR HESITANCY OR HESITATION? ? OR HIATUS OR HI-NDER?? OR HOLD??? OR INTERIM OR INTERLUDE? ? OR INTERMISSION-?? OR INTERRUPTION? ?
S16 151 S14 OR S15
S17 52 CONSTANT? OR PERMANENT? OR REGULAR? OR STABILE OR STABLE OR STEADFAST OR STEADY OR UNBROKEN OR UNCHANG? OR UNFLUCTUAT? -OR UNIFORM? OR UNINTERRUPT? OR UNVARY?
S18 9 S16 (15N) S17
S19 21 S12 OR S18
S21 122 (REGISTER? OR MEMORY OR STORE? ? OR STORING OR STORAGE) (-9N) (ACTIVE OR ACTIVAT??? OR CURRENT??? OR TOP OR FRONT OR F-OCUS? OR SELECT???)
S22 132 S19 OR S21
S23 113 S22 AND PY=1963:2002
S24 100 S22 AND AY=1963:2002
S25 120 S23 OR S24
S26 424 CLOCK
S27 120 S25 AND S26
S28 120 IDPAT (sorted in duplicate/non-duplicate order)
S29 120 IDPAT (primary/non-duplicate records only)
S30 82 (REGISTER? OR MEMORY) (9N) (ACTIVE OR ACTIVAT??? OR CURRE-NT??? OR TOP OR FRONT OR FOCUS? OR SELECT???)
S31 96 S19 OR S30
S32 81 S31 AND PY=1963:2002
S33 424 CLOCK

S34 81 S32 AND S33
S37 22 PIPELIN?
S38 7 S34 AND S37
S39 7 IDPAT (sorted in duplicate/non-duplicate order)
S40 7 IDPAT (primary/non-duplicate records only)
S41 74 S34 NOT S38
S42 6 LATENCY
S43 2 S41 AND S42
S44 2 SWAP?
S45 2 S44 NOT S38
S46 9 41 NOT S45
S47 74 S41 NOT S45

40/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0012456054 - Drawing available
WPI ACC NO: 2002-401958/200243
XRPX Acc No: N2002-315107
Pipeline for processing instruction in microcontroller used in microwave oven, television, transmits read address to SRAM based on modified value in address pointer
Patent Assignee: SCENIX SEMICONDUCTOR INC (SCEN-N)
Inventor: CHENG C C
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 6353880	B1	20020305	US 1998121224	A	19980722	200243 B

Priority Applications (no., kind, date): US 1998121224 A 19980722

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 6353880	B1	EN	16	9	

Pipeline for processing instruction in microcontroller used in microwave oven, television, transmits read address to SRAM based on modified value in address pointer

Original Titles:
Four stage **pipeline** processing for a microcontroller.

Alerting Abstract ...which in turn is coupled to write data output of a write back stage (160), so as to transmit the calculation results in the corresponding **clock** cycle, to the execution stage. Another control logic generates and transmits the read address to a SRAM (120), based on the modified value in an...
...USE - For processing instruction in microcontroller used in microwave oven, television, calculator, remote control, **clock**, etc...

...ADVANTAGE - The instructions are executed efficiently for each **clock** cycle, without requiring use of expensive hardware. Instruction processing speed is enhanced...

Original Publication Data by Authority

Original Abstracts:
A system and method for efficiently processing instructions in a

pipeline architecture for a microcontroller and maintaining a fixed instruction execution per clock cycle rate is disclosed. The pipeline comprises four stages: an instruction fetch stage, an operand fetch stage, an execution stage, and a write back stage. In a first embodiment, an entire clock cycle is dedicated to the instruction fetch stage to the instruction fetch stage to retrieve instruction data from non-volatile memory in a single clock cycle. In a second embodiment, the operand fetch stage preliminarily decodes the instruction data to determine tasks to be performed to allow the execution stage to perform its time-intensive calculations in a single clock cycle. Additionally, the operand fetch stage initiates the performance of tasks determined from the decoding of the instructions to minimize the time required to perform...

...port data memory is employed to allow the execution stage and the write back stage to perform read and write operations concurrently, in a single clock cycle. Additional embodiments are disclosed for addressing circumstances in which one stage modifies the data address pointer required by another stage or one stage writes to an data memory location required for a read operation by a previous stage. Thus, a one instruction per clock cycle rate is achieved and maintained.
Claims:
A pipeline for processing instructions for a microcontroller in four stages, wherein operations in each stage are performed concurrently in a single clock cycle, comprising:data memory for retrieving data in response to receiving a read address and storing data in response to receiving a write address, said data memory...

...execution stage, the data memory, and the write back stage, for comparing the write address and the read address of consecutive instructions in a first clock cycle and, responsive to the write address and the read address of consecutive instructions being identical,transmitting a disable signal to an enable input of the data memory to disable a read operation, and coupling a write data register to the write data output for storing a copy of the results of the calculations in the first clock cycle; and,coupling the read input of the execution stage to the write data register to transmit the stored copy of the results of the calculations to the execution stage in a second instruction cycle occurring after said first instruction cycle; anda second conditional...

...data memory, and the write back stage, for, responsive to a first instruction modifying a value in the data address pointer and a second instruction performing a read operation, selecting the modified value, generating a read address responsive to the modified value, and transmitting the generated read address to the data memory.>

40/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0011151515 - Drawing available
WPI ACC NO: 2002-088672/200212
XRPX Acc No: N2002-065276
Interrupt handling system in microcontrollers, copies and restores program and memory address data into shadow and primary registers within one clock cycle of interrupt enter and exit signals
Patent Assignee: SCENIX SEMICONDUCTOR INC (SCEN-N)
Inventor: CHENG C C
Patent Family (1 patents, 1 countries)
Patent Application

Number Kind Date Number Kind Date Update
US 6243804 B1 20010605 US 1998121201 A 19980722 200212 B

Priority Applications (no., kind, date): US 1998121201 A 19980722

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 6243804 B1 EN 14 7

Interrupt handling system in microcontrollers, copies and restores program and memory address data into shadow and primary registers within one **clock** cycle of interrupt enter and exit signals

Original Titles:
Single cycle transition **pipeline** processing using shadow registers.

Alerting Abstract ...104). On completion of ISR, copied contents are restored back into primary registers. Copying and restoring of address and memory data take place within one **clock** cycle of respective interrupt enter and exit signals....program and memory addresses into shadow registers on initiation of ISR and restoring back of copied addresses on completion of ISR take place within one **clock** cycle of interrupt enter and exit signals, the ISR is able to immediately execute event handling instructions and is able to more quickly return control...

Title Terms.../Index Terms/Additional Words: **CLOCK**;

Original Publication Data by Authority

Original Abstracts:
A system and method for efficiently handling interrupts in a microcontroller environment is disclosed. An interrupt handling circuit preserves a **current** state of a microcontroller comprising a plurality of primary **registers** for storing information relating to the **current** state of the microcontroller and a plurality of shadow **registers** coupled to at least two of the primary registers for storing the information contained in the coupled primary registers in response to receiving an interrupt...

...data, CPU status data, and an address pointer to data memory. In a preferred embodiment, the information is restored to the primary registers within one **clock** cycle of receiving an interrupt exit signal from the interrupt signal generator. In a **pipeline** stage embodiment a sequence of interrupt instructions is fed into the **pipeline** in subsequent **clock** cycles after the data is stored in the shadow registers, facilitating a rapid response to the interrupt.
Claims:
...for generating an interrupt enter signal responsive to an external event;means for initiating an interrupt service routine in response to the interrupt enter signal;**pipeline** means having a plurality of stages coupled **to** a memory for processing instructions;means for coupling a first primary register containing program address data to a corresponding shadow register responsive to receiving the...

...to receiving the generated interrupt enter signal;interrupt service routine means for entering a first interrupt service routine of an interrupt service routine into the **pipeline** means responsive to the generated interrupt enter signal;interrupt signal generator logic circuit means for generating an interrupt exit signal responsive **to** completion of the interrupt service routine;responsive to receiving the

generated interrupt exit signal, means for coupling the first primary register to the corresponding shadow...

...primary registers; andmeans for decoupling the corresponding registers from the coupled primary registers;whereby the contents of the primary registers are stored within one **clock** cycle of the interrupt enter cycle and restored within one **clock** cycle of the interrupt exit signal. Basic Derwent Week: **200212**

40/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008851562 - Drawing available
WPI ACC NO: 1998-398520/**199834**
Related WPI Acc No: 1997-258512; 1997-448253; 1997-549283; 1998-086484; 2002-582101
XRPX Acc No: N1998-310077
Dynamic **pipeline** for microprocessor - includes control logic that controls first data selector to select either first set of data or first operation data as selected data
Patent Assignee: CIRRUS LOGIC INC (CIRR-N)
Inventor: DYE T A
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 5778250	A	19980707	US 1994247657	A	19940523	199834 B
			US 1997854654	A	19970512	

Priority Applications (no., kind, date): US 1994247657 A 19940523; US 1997854654 A 19970512

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5778250	A	EN	15	4	Continuation of application US 1994247657

Dynamic **pipeline** for microprocessor...

Original Titles:
Method and apparatus for dynamically adjusting the number of stages of a multiple stage **pipeline**.

Alerting Abstract ...The **pipeline** includes a first circuit for providing a first set of data. A first latch connected to the first circuit receives the **clock** signal for providing latched copy of the first set of data during each cycle of **clock** signal. A second circuit provides a second set of data. A second latch connected to the second circuit receives the **clock** signal for providing a latched copy of the second set of data during each cycle of the **clock** signal. A first operation element connected to the first latch and the second latch for performing first operation using the latched copy of the first...

...to select either the first set of data or first operation data as selected data. A third latch connected to the data selector receives the **clock** signal for providing latched copy of the **selected** data. A third circuit includes a **register** for storing offset value...

...A second data **selector** has a first input that is connected to the **register** and the second input that is connected to a second operation

element for receiving second operation data. The output of the second data selector generates third set of data. The control logic controls the second data selector to alternately select output of register and the second operation element on consecutive cycles of the clock signal. A fourth latch is connected to the third circuit and receives clock signal for providing latched copy of the third set of data during each cycle of the clock signal. The second operation element is connected to the third and the fourth latches for performing a second operation using latched copy of the selected...

Original Publication Data by Authority

Original Abstracts:
A dynamic pipeline for a processor, including multiple latch stages for providing data to corresponding operation elements and multiplexers with associated control logic for bypassing one or more latch stages and operation...
Claims:
A dynamic pipeline receiving a clock signal, comprising: a first circuit for providing a first set of data; a first latch coupled to said first circuit and receiving the clock signal for providing a latched copy of said first set of data during each cycle of the clock signal; a second circuit for providing a second set of data; a second latch coupled to said second circuit and receiving the clock signal for providing a latched copy of said second set of data during each cycle of the clock signal; a first operation element coupled to said first latch and said second latch for performing a first operation using said latched copy of said first set of data and said latched copy of said...

...said first set of data or said first operation data as said selected data; a third latch coupled to said data selector and receiving the clock signal for providing a latched copy of said selected data from said data selector; a third circuit for providing a third set of data, including: a register for holding an offset value; and a second data selector having a first input coupled to said register and a second input coupled to said second operation element for receiving said second operation data, and an output for providing said third set of data, said control logic controlling said second data selector to alternately select between said register and said second operation element on consecutive cycles of the clock signal; a fourth latch coupled to said third circuit and receiving the clock signal for providing a latched copy of said third set of data during each cycle of said clock signal; and a second operation element coupled to said third and fourth latches for performing a second operation using said latched copy of said selected data and said latched copy of said third set of data as operands, and for providing second operation data. ...

40/3,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008802830 - Drawing available
WPI ACC NO: 1998-347906/199830
XRPX Acc No: N1998-271596
Superscalar microprocessor system with way prediction function - has selection control bits stored in way prediction storage unit that indicates selection of stored branch prediction address and additional address during first and second state respectively

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: PICKETT J K; TRAN T M
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5764946	A	19980609	US 1995420641	A	19950412	199830 B
			US 1997826884	A	19970408	

Priority Applications (no., kind, date): US 1995420641 A 19950412; US 1997826884 A 19970408

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5764946	A	EN	136	68	Continuation of application US 1995420641

Alerting Abstract ...prediction unit with a first input port. The first input port is configured to convey an input address and an update value during a first **clock** cycle. The update value includes an update way value. A way prediction storage unit coupled to the input port includes a set of storage locations...

...an output way value. The branch prediction unit provides a branch prediction address from one among the multiple storage locations, as output address during first **clock** cycle. The way value from the storage locations is output as output way value during first **clock** cycle...

...provided for storing previously fetched instruction blocks. The instruction cache which comprises multiple memory blocks receives the input address and output way value during first **clock** cycle. One of the **memory** blocks in the instruction cache is **selected** corresponding to the input address and the output way value. A fetch PC unit coupled to the instruction cache and the branch prediction unit receives the output address and conveys it as input address to the first input port during second **clock** cycle succeeding first **clock** cycle. The storage locations in the way prediction storage unit stores one additional address and multiple selection control bits. The selection control bits indicates selection...

...ADVANTAGE - Enables fetching of instruction in one **clock** cycle.

Original Publication Data by Authority

Original Abstracts:
...read from the instruction cache. The microprocessor may achieve high frequency operation while using an associative instruction cache. An instruction fetch can be made every **clock** cycle using the **predicted** fetch address from the way prediction unit until an incorrect next fetch address or an incorrect way is predicted. The instructions from the predicted way are provided to the instruction processing **pipelines** of the superscalar **microprocessor** each **clock** cycle.
Claims:
...prediction unit, wherein said instruction cache is configured to provide said fetch address to said branch prediction unit, and wherein said instruction cache is configured **to** select one of a plurality **of** memory **blocks** included within said instruction cache **according** to an index of said fetch address and said one of said plurality of way predictions, and wherein said instruction cache is configured to subsequently...

40/3,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007699835 - Drawing available
WPI ACC NO: 1996-321981/**199632**
XRPX Acc No: N1996-270897
Low power filter coefficient adaptation circuit for digital adaptive filter
- uses independent clocking for adaptive filter and adaptation circuitry, such that input and output data samples are clocked through adaptive filter at higher rate to that used to update filter coefficients
Patent Assignee: QUANTUM CORP (QUAN)
Inventor: ABBOTT W L; NGUYEN H C
Patent Family (5 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
WO 1996020450	A1	19960704	WO 1995US15849	A	19951206	199632 B
EP 804768	A1	19971105	EP 1995942560	A	19951206	199749 E
			WO 1995US15849	A	19951206	
US 5734598	A	19980331	US 1994367028	A	19941228	199820 E
JP 10511797	W	19981110	WO 1995US15849	A	19951206	199904 E
			JP 1996520461	A	19951206	
KR 1998701110	A	19980430	WO 1995US15849	A	19951206	199914 E
			KR 1997704454	A	19970627	

Priority Applications (no., kind, date): US 1994367028 A 19941228

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
WO 1996020450	A1	EN	22	8	
National Designated States,Original: JP KR SG					
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
EP 804768	A1	EN			PCT Application WO 1995US15849
					Based on OPI patent WO 1996020450
Regional Designated States,Original: DE FR GB IT NL					
US 5734598	A	EN	15	8	
JP 10511797	W	JA	28		PCT Application WO 1995US15849
					Based on OPI patent WO 1996020450
KR 1998701110	A	KO			PCT Application WO 1995US15849
					Based on OPI patent WO 1996020450

Alerting Abstract ...independently clocked from the adaptation circuit (48), such that input data samples and the processed output data samples are clocked through the filter at a **clock** rate (1/T), and the filter coefficients are updated according to a prescribed algorithm at an update rate slower that the 1/T **clock** rate. Filter coefficient updating occurs pref at a rate equal to 1/J, where J is an integer greater than unity, (between 2 and 8), and the coefficient update rate is achieved by providing a separate filter coefficient adaptation **clock** (49) derived from the system **clock**, by dividing the **clock** by a user programmable parameter (J...

Title Terms.../Index Terms/Additional Words: **CLOCK**;

Original Publication Data by Authority

Original Abstracts:

...from the adaptation circuitry (48), such that the input data samples and the processed output data samples are clocked through the adaptive filter at a clock rate 1/T, and the filter coefficients are updated according to a prescribed algorithm at an update rate slower than the 1/T clock rate.Filter coefficient updating occurs preferably at a rate equal to 1/J, where J is an integer greater than unity and generally in the range of 2 to 8. The coefficient update rate is achieved by providing a separate filter coefficient adaptation clock (49) derived from the system clock by dividing that clock by a user-programmable parameter J. This process reduces the coefficient update rate, which in turn reduces the switching frequency of the logic gates, the number of pipeline latches, and, ultimately, the power consumption...clocked from the adaptation circuitry, such that the input data samples and the processed output data samples are clocked through the adaptive filter at a clock rate 1/T, and the filter coefficients are updated according to a prescribed algorithm at an update rate slower than the 1/T clock rate. Filter coefficient updating occurs preferably at a rate equal to 1/J, where J is an integer greater than unity and generally in the range of 2 to 8. The coefficient update rate is achieved by providing a separate filter coefficient adaptation clock derived from the system clock by dividing that clock by a user-programmable parameter J. This process reduces the coefficient update rate, which in turn reduces the switching frequency of the logic gates, the number of pipeline latches, and, ultimately, the power consumption.

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Claims:

...independently clocked from the adaptation circuit (48), such that input data samples and the processed output data samples are clocked through the filter at a clock rate (1/T), and the filter coefficients are updated according to a prescribed algorithm at an update rate slower that the 1/T clock rate. Filter coefficient updating occurs pref at a rate equal to 1/J, where J is an integer greater than unity, (between 2 and 8), and the coefficient update rate is achieved by providing a separate filter coefficient adaptation clock (49) derived from the system clock , by dividing the clock by a user programmable parameter (J...unity and said digital adaptation unit is structured and arranged not to update said coefficients otherwise, and wherein said digital adaptation unit comprises:a first clock providing the clocking period T governing the rate of operation of said filter;an adaptation clock providing an adaptation clocking period JT governing the rate of operation of said digital adaptation unit,error generator means for providing error values for use in updating said filter coefficients;error value storing means connected to said error generator means for storing said error values, wherein said error value storing means provides stored error values for use in said updating in response to said adaptation clock,error scaling means receiving said stored error value from said error value storing means in response to said adaptation clock signal for scaling

said error value by a selectable step size for use in said updating, andstep size selector means for providing a selected step size to said shift register such that a larger step size is selected for a faster filter coefficient adaptation mode and a smaller step size is selected for a slower filter coefficient adaptation mode. ...
Basic Derwent Week: 199632...

40/3,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007468776 - Drawing available
WPI ACC NO: 1996-079507/199609
Related WPI Acc No: 1994-009121; 1995-346814; 1998-365305; 1999-073218; 1999-073220; 1999-073219; 1999-083979; 1999-073222; 1999-073221; 1999-073217; 1996-173495; 1995-360866; 1995-346813; 1995-322700; 1995-322737
XRPX Acc No: N1996-066149
MPEG decompression apparatus for audio and video signals - uses serial pipeline processing system with single two-wire bus carrying control and DATA tokens
Patent Assignee: DISCOVISION ASSOC (MCAC)
Inventor: ANDREW P K; BARNES D A; BARNES M; BIRCH N; CLAYDON A P J; DEWAR K D; FINCH H R; JONES A M; KULIGOWSKI A P; MARK B; MARTIN W S; PATTERSON D W; PATTERSON D W W; ROBBINS W P; SMITH C; SOTHERAN M W; WISE A P
Patent Family (31 patents, 21 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 695095	A2	19960131	EP 1995305308	A	19950728	199609 B
AU 199525019	A	19960208	AU 199525019	A	19950717	199613 E
CA 2154962	A	19960130	CA 2154962	A	19950728	199620 E
JP 8172624	A	19960702	JP 1995224473	A	19950728	199636 E
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			US 1995481785	A	19950707	
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			US 1995481772	A	19950607	
US 5768629	A	19980616	US 199382291	A	19930624	199831 E
			US 1995382958	A	19950202	
			US 1995400201	A	19950307	
			US 1995400397	A	19950307	
			US 1995473813	A	19950607	
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US 1997991234 A 19971216
SG 108204 A1 20050128 SG 1995986 A 19950729 200523 E
MX 199901886 A1 20040901 MX 19991886 A 19990225 200556 E

...uses **serial pipeline** processing system with single two-wire bus carrying control and DATA tokens

Alerting Abstract ...The apparatus uses stages interconnected by a two-wire interface arranged as a **pipeline** processing machine. A staged token decode circuit recognises control tokens pertinent to a particular stage and passes unrecognised control tokens along the **pipeline**. Reconfiguration processing circuits in some stages are

responsive to a recognised token for reconfiguring the stage to handle an identified DATA token...

Title Terms.../Index Terms/Additional Words: SERIAL;

Original Publication Data by Authority

Original Abstracts:
An MPEG video decompression method and apparatus utilizing a plurality of stages interconnected by a two-wire interface arranged as a pipeline processing machine. Control tokens and DATA Tokens pass over the single two-wire interface for carrying both control and data in token format. A token decode circuit is positioned...

...certain of the stages for recognizing certain of the tokens as control tokens pertinent to that stage and for passing unrecognized control tokens along the pipeline. Reconfiguration processing circuits are positioned in selected stages and are responsive to a recognized control token for reconfiguring such stage to handle an identified DATA Token. A wide variety...

...An MPEG video decompression method and apparatus utilizing a plurality of stages interconnected by a two-wire interface arranged as a pipeline processing machine. Control tokens and DATA Tokens pass over the single two-wire interface for carrying both control and data in token format. A token decode circuit is positioned in certain of the stages for recognizing certain of the tokens as control tokens pertinent to that stage and for passing unrecognized control tokens along the pipeline. Reconfiguration processing circuits are positioned in selected stages and are responsive to a recognized control token for reconfiguring such stage to handle an identified DATA Token. A wide variety of unique supporting subsystem circuitry...

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...memory addressing, transforming data using a common processing block, time synchronization, asynchronous swing buffering, storing of video information, a parallel Huffman decoder, and the like.

Claims:
1. An apparatus for synchronizing time, comprising:</br> a time stamp for determining presentation time;</br> a **clock** reference for initializing system time **in** a first **circuit**;</br> a first time counter in **communication** with said **clock** reference for **keeping** system time in a **first circuit**; and</br> **a** second time counter initialized by **said clock** reference , in a second circuit synchronized with said first **time** counter, for **keeping** a local **copy** of said system time and for **determining** the presentation **timing** error between said local **copy** of system time and said system time by comparing **said** time stamp to said second time counter...

...An apparatus for synchronizing a system decoder and a video decoder, comprising:a system decoder;a time stamp for determining display time;a **clock** reference for initializing system time in said system decoder;a first time counter in communication with said **clock** reference **for** keeping system time in said system decoder; anda second time counter initialized by said **clock** reference in said **video** decoder synchronized with said first time counter, for keeping a local copy of system time and for determining the **display** timing error between said local copy of system time and said system time by comparing the time stamp to said second time counter...

...A **pipelined** video decoder system having an input, an output and a plurality of processing stages therebetween, and receiving an input stream of encoded data comprising:a token generator, responsive to **a** picture start code and to extension start code identifiers and user data in the input stream for generating a universal adaptation unit in the form of an interactive interfacing token for control and/or data functions among said processing stages, wherein said interactive interfacing token is **serially** transmitted through said processing stages;wherein a discard--user configuration bit is included in a data packet of the input stream; and a discard--extn bit is included in the data **packet**;

wherein responsive to a first condition of said discard extn bit the token generator disregards the extension start code identifier, and responsive to a second condition of said discard--extn bit the extension start code identifier is replaced with another extension data token;whereby extension and user data are selectively specified for the user by the processing system.

A pipelined video decoder system having an input, an output and a plurality of processing stages therebetween, comprising:a universal adaptation unit in the form of a first interactive interfacing token for control and/or data functions among said processing stages;a token generator, responsive to a picture start code in an input stream of encoded data for generating said first interactive interfacing token, wherein said first interactive interfacing token is serially transmitted through said processing stages;wherein said first interactive interfacing token is a GROUP--START token for indicating a start of a group sequence; and...

...generation of said GROUP--START token, said token generator generates a second interactive metamorphic interfacing token comprising a PICTURE--END token, said PICTURE--END token being serially transmitted to said processing stages before data associated with said start code is output, wherein responsive to said PICTURE--END token one of said processing...

...operation, and said one processing stage generates a FLUSH token in a second mode of operation, wherein processing of said current picture is completed in a controlled manner...

...A parallel Huffman decoder, accepting a mixed data stream comprising Huffman coded variable length codes, and fixed length codes comprising:a selector operative on said data stream:a pair of input registers for receiving Huffman coded data, both of said registers directing input in parallel to said selector; anda Huffman Code ROM for receiving input from said selector and a ROM table select input; said Huffman Code ROM providing decoded data output...

...variable length codes are provided by said selector to said Huffman Code ROM, and in a second mode of operation a signal representative of a length of fixed length codes is output from said selector without being provided to said Huffman Code ROM.ol>A method for operating a state machine, comprising the steps of:providing an arithmetic core having a data stream flowing therethrough;providing a memory linked to said arithmetic core and installing a plurality of microcode instructions in said memory;controlling the operation of the arithmetic core according to the microcode instructions to modify the data stream;addressing the memory to select said microcode instructions for execution thereof by providing an address word having a predetermined fixed number of bits;defining the fixed width word with...

...least one bit to serve as a termination marker between the address field and the substitution field;using the substitution field to indicate substituted bits from a separate addressing source; andmaintaining the fixed width word while inversely varying the width of the address field and the width of the substitution field...

...fixed length codes is output by the decoder without reference to said ROM;a pair of input registers for receiving Huffman coded data, both of said registers directing input in parallel to said selector; anda Huffman Code ROM for receiving input from said selector and another ROM table select input; said ROM providing a first decoded data...

...A pipelined video decoder system having an input, an output and a plurality of processing stages therebetween, comprising:a universal adaptation unit in the form of a first interactive interfacing token for control and/or data functions among said processing stages;a start code detector, responsive to a picture start code in an input...

...comprising MPEG data;a token generator, responsive to said start code detector for generating said first interactive interfacing token, wherein said first interactive interfacing token is serially transmitted through said processing stages;wherein said processing stages comprise electrical circuits, and said picture start code comprises an MPEG2 extension--start--code--identifier, and said first interactive interfacing token is a SEQUENCE--EXTN token for indicating sequence extension identification.

...

...and a second buffer defined therein;a write control circuit in communication with said memory array through bit lines;a read control circuit in communication with said memory array through bit lines;a read row decoder and a write row decoder;a plurality of wordlines, each said wordline being in communication...

...each wordline of said second pair being assigned a single write address by said write row decoder;a first selector in said read row decoder for selecting one of said wordlines of said first pair, whereby said first buffer is accessed at said read address;a second selector in said write row decoder for selecting one of said wordlines of said second pair, whereby said second buffer is accessed at said write address;a first control line interconnecting said read control circuit and said write control circuit having a first signal thereon that is indicative of a selected wordline of said first pair; anda second control line interconnecting said read control circuit and said write control circuit having a second signal thereon that is indicative of a ol>In a pipelined video decoder and decompression system having an input, an output and a plurality of processing stages between the input and the output:a...

...to an MPEG2 extension start code in an input stream of encoded data for generating said first interactive interfacing token, wherein said first interactive interfacing token is serially transmitted through said processing stages;wherein said processing stages comprise a temporal decoder responsive to tokens generated by said first token generator, and ..:

...and comprising:a first frame store for storage of a first video frame;a second frame store for storage of a second video frame; anda third frame store having defined therein a first field store and a second field store therein, a third video frame being stored in a selected...

...For use with a system having a plurality of pipelined processing stages:a data path serially connecting said pipelined processing stages for carrying data received by the system and carrying control information;a universal adaptation unit in the form of an interactive...

...stages are disabled by said microprogrammable state machine.

In a video decoding...

...Huffman coded variable length codes, and having data stored therein

representing decoded data and information representative of a length of the Huffman coded variable length codes;a selector, responsive to an output of said memory, wherein in a first mode of operation variable length codes are provided to said memory address lines, and in a second mode of...

...second frame store; providing a third frame store having a first and a second field store, the first and second field stores each defining first and second subfield stores;storing the third frame in a selected portion of the memory area in the first or second field store;while performing said step of storing the third frame reading a portion of said stored third frame from the selected portion of the memory;thereafter writing a portion of the fourth frame into the selected portion of the memory area....a plurality of elementary streams of data, each said elementary stream comprising a series of access units and having a series of time stamps associated therewith;a clock reference for initializing system time in a first circuit;a first time counter in communication with said clock reference for keeping system time in a first circuit; anda second time counter initialized by said clock reference in a second circuit synchronized with said first time counter, for keeping a local copy of said system time and for determining the presentation timing error between said local copy of system time and said system time by comparing said time stamp to said second time counter.

A method for addressing memory, comprising the steps of:providing a fixed width word having a predetermined fixed number ...

...a termination marker between the address field and the substitution field;using the substitution field to indicate substituted bits from a separate addressing source; andmaintaining a fixed width word for addressing variable width data while inversely varying the width of the address field and the width of the substitution field.

...

...a write address to said write row decoder, said write address encoding said row address;decoding said read address;selecting one of said first row and said second row for reading to define a first selected row;decoding said write address;asynchronous with said step of selecting one of said first row and said second row for reading, selecting one of said first row and said second row for writing to define a second selected row;reading data from a first storage location of said first selected row;asynchronous with said step of reading data, writing data into a second storage location of said second selected row; andsignaling to identify said first selected row and signaling to identify said second selected row to coordinate said steps of ...

Basic Derwent Week: 199609...

40/3,K/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005338885 - Drawing available
WPI ACC NO: 1990-337216/199045
XRPX Acc No: N1990-257891
Stack method and circuitry - decodes instruction requiring stack push operation and generates control indicator calling for stack push operation

Patent Assignee: INTEL CORP (ITLC)
Inventor: SAINI A
Patent Family (5 patents, 4 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
GB 2231181	A	19901107	GB 19903475	A	19900215	199045 B
FR 2645663	A	19901012				199048 E
US 5142635	A	19920825	US 1989334920	A	19890407	199237 E
GB 2231181	B	19930421	GB 19903475	A	19900215	199316 E
IE 63907	B	19950614	IE 19901209	A	19900403	199531 E

Priority Applications (no., kind, date): US 1989334920 A 19890407

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5142635	A	EN	20	6	
IE 63907	B	EN			

Original Titles:
Method and circuitry for performing multiple stack operations in succession in a **pipelined** digital computer

Alerting Abstract ...In the system during a first **clock** cycle, an instruction is decoded requiring a stack push operation. A control indicator is also generated calling for a stack push operation. During a phase one of a second **clock** cycle, (a) a stack pointer value stored in a first stack pointer register is written onto a first bus, and (b) the stack pointer value stored in the first stack pointer register is written into an input latch of a stack pointer adder. During a phase two of the second **clock** cycle, (a) a stack memory address is formed by using the stack pointer value on the first bus, (b) the stack pointer value stored in ...

...During a phase one of a third **clock** cycle, (a) the updated stack pointer value stored in the output latch is written onto a second bus, and (b) the updated stack pointer value on the second bus is written into a second stack pointer register for storage. During a phase two of the third **clock** cycle, (a) data is written to memory for storage at a memory location indicated by the stack memory address, and (b) the updated stack pointer...

...ADVANTAGE - Reduced number of **clock** cycles Permits overlapping of successive stack operations. @(49pp DWg.No.2/6)@

Equivalent Alerting Abstract ...to push data onto a stack in memory comprises decoding an instruction requiring a stack push operation and generating a control indicator during a first **clock** cycle. During phase one of a second **clock** cycle a selected stack pointer value is written onto a bus and an input latch of a stack pointer adder. During phase two a stack...

...During a phase one of a third **clock** cycle the updated pointer value is written onto a second bus and stored in a second stack pointer register. During a phase two of the third **clock** cycle the data is written to a memory location indicated by the stack memory address and the updated stack pointer value is stored in the...

...ADVANTAGE - Reduced number of **clock** cycles required to perform stack operation. Executes stack push or pop operation in one **clock** cycle. Can perform back-to-back stack operations in digital computer with **pipelined** instructions.

Original Publication Data by Authority

Original Abstracts:
A method for performing consecutive instructions to push data onto a stack in memory in a digital computer is described. During a first **clock** cycle, an instruction is decoded requiring a stack push operation. A control indicator is also generated calling for a stack push operation. During a phase one of a second **clock** cycle, (a) a stack pointer value stored in a **selected** stack pointer **register** is written onto a first bus, the **selected** stack pointer **register** being one of either the first stack pointer register or the second stack point **register**, and (b) the stack pointer value stored in the **selected** stack pointer **register** is written into an input latch of a stack pointer adder. During a phase two of the second **clock** cycle, (a) a stack memory address is formed by using the stack pointer value on the first bus, (b) the stack pointer value stored in...

...an updated stack pointer value, and (c) the updated stack pointer value is stored in an output latch. During a phase one of a third **clock** cycle, (a) the updated stack pointer value stored in the output latch is written onto a second bus, and (b) the updated stack pointer value on the second bus is written into a second stack pointer register for storage. During a phase two of a third **clock** cycle, (a) data is written to memory for storage at a memory location indicated by the stack memory address, and (b) the updated stack pointer...
Claims:
In the system during a first **clock** cycle, an instruction is decoded requiring a stack push operation. A control indicator is also generated calling for a stack push operation. During a phase one of a second **clock** cycle, (a) a stack pointer value stored in a first stack pointer register is written onto a first bus, and (b) the stack pointer value stored in the first stack pointer register is written into an input latch of a stack pointer adder. During a phase two of the second **clock** cycle, (a) a stack memory address is formed by using the stack pointer value on the first bus, (b) the stack pointer value stored in...

...During a phase one of a third **clock** cycle, (a) the updated stack pointer value stored in the output latch is written onto a second bus, and (b) the updated stack pointer value on the second bus is written into a second stack pointer register for storage. During a phase two of the third **clock** cycle, (a) data is written to memory for storage at a memory location indicated by the stack memory address, and (b) the updated stack pointer...

...1) during a first **clock** cycle, decoding an instruction requiring a stack push operation and generating a control indicator calling for a stack push operation...
...2) during a phase one of a second **clock** cycle, performing steps comprising...

...a) writing onto a first bus stack pointer value stored in a **selected** stack pointer **register**, the **selected** stack pointer **register** being one of a first stack pointer register and a second stack pointer register...

...b) writing the stack pointer value stored in the **selected** stack pointer **register** into an input latch of a stack pointer adder...

...3) during a phase two of the second **clock** cycle, performing steps

comprising...

...4) during a phase on of a third **clock** cycle, performing steps comprising...

...5) during a phase two of the third **clock** cycle, performing steps comprising...
Basic Derwent Week: **199045**

45/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0004800986 - Drawing available
WPI ACC NO: 1989-172932/198923
Exchange scan testing of digital logic - has operational multiplexer coupled to receive operational data at one input and stored test data at other input
Patent Assignee: RAYTHEON CO (RAYT)
Inventor: TERZIAN J
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 4831623	A	19890516	US 198774101	A	19870716	198923 B

Priority Applications (no., kind, date): US 198774101 A 19870716

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 4831623	A	EN	13	6	

Original Titles:
Swap scan testing of digital logic
Alerting Abstract ...A **swapper** is responsive to a test control signal, for coupling the output of the operational register into the input of the test register and for coupling the output of the test register into the input of the operational register for **swapping** the stored operational data and stored test data...

Original Publication Data by Authority

Original Abstracts:
Apparatus and method for dynamically testing logic circuits transparent to their normal operation without placing restrictions on the logic circuit design. The apparatus is a **swap** scan register including an operational register for storing operational data and a test register for storing test data. The operational and test registers operate independently of each other. A **swap** circuit enables exchanging the operational and test register contents. According to the method disclosed after test data is stored in the test register, the operational register is interrupted and its contents **swapped** with the test register for one clock cycle. The test and operational registers are then **swapped** again to restore the original operational data to its pre-interrupt state and to provide test results in the test register.

47/3,K/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO

03403190 **Image available**
MEMORY CIRCUIT

PUB. NO.: 03-066090 [JP 3066090 A]
PUBLISHED: March 20, 1991 (**19910320**)
INVENTOR(s): NATORI KENJI

APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-201365 [JP 89201365]
FILED: August 04, 1989 (19890804)
JOURNAL: Section: P, Section No. 1213, Vol. 15, No. 226, Pg. 44, June 10, 1991 (19910610)

...PUBLISHED: **19910320)**

ABSTRACT

PURPOSE: To prevent destruction of stored information of non-access cell at accessing by providing a means controlling in common a storage means of a **memory** cell connecting to a word line receiving a **selection** signal...

... TR) 1-1 connecting to a word line W(sub 1) and a bit line B(sub 1) and write operation is implemented, then a **clock** pulse is given from an address decoder 4 to a drive line D(sub 1) from an address decoder 4 and applied also to a...

... capacitor 3' is inverted by the readout operation and since the data of the same level as that stored so far is rewritten when the **clock** pulse is applied, the its own polarization restores and the destruction of a stored data is prevented.

47/3,K/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

01774448 **Image available**
ARITHMETIC PROCESSOR

PUB. NO.: 60-252948 [JP 60252948 A]
PUBLISHED: December 13, 1985 **(19851213)**
INVENTOR(s): SAITO KOJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-109063 [JP 84109063]
FILED: May 29, 1984 (19840529)
JOURNAL: Section: P, Section No. 455, Vol. 10, No. 127, Pg. 95, May 13, 1986 (19860513)

...PUBLISHED: **19851213)**

ABSTRACT

... with execution of an instruction of an arithmetic unit 2 is transmitted to buffer registers 301-302 respectively and then shifted successively according to the **clock** cycles. While the instructions are designated successively by a register group 1 and transmitted in response to the **clock** cycle. If the instructions are continuous for replacement of the same operand stored in the group 1, the data that replaces the subsequent instructions is defined as the latest data of the group 1. Thus a **selection** means 4 **selects** the data held by a **register** of a younger number among those buffer registers 301-303.

47/3,K/18 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0012799057 - Drawing available

WPI ACC NO: 2002-655656/200270
Related WPI Acc No: 2002-179047; 2002-179048; 2002-179220; 2002-179222; 2002-443510; 2002-443512; 2002-617869; 2002-722945; 2003-039635; 2003-331594; 2003-786619; 2004-339483; 2004-410254; 2004-603011; 2005-073591
XRPX Acc No: N2002-518136
Protocol engine for multiprocessor computer system, copies instruction corresponding to instruction address from cache to instruction latch in next clock cycle which is not associated with current clock cycle
Patent Assignee: BARROSO L A (BARR-I); GHARACHORLOO K (GHAR-I); HEWLETT-PACKARD DEV CO LP (HEWP); RAVISHANKAR M K (RAVI-I); STETS R J (STET-I)
Inventor: BARROSO L A; GHARACHORLOO K; RAVISHANKAR M K; STETS R J
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20020087806	A1	20020704	US 2000210675	P	20000610	200270 B
			US 2001878982	A	20010611	
			US 200242029	A	20020107	
US 6622218	B2	20030916	US 200242029	A	20020107	200362 E

Priority Applications (no., kind, date): US 2001878982 A 20010611; US 2000210675 P 20000610; US 200242029 A 20020107

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20020087806	A1	EN	75	31	Related to Provisional US 2000210675 C-I-P of application US 2001878982

Protocol engine for multiprocessor computer system, copies instruction corresponding to instruction address from cache to instruction latch in next clock cycle which is not associated with current clock cycle

Alerting Abstract ...NOVELTY - A scheduler selects a active memory transaction from an array during current clock cycle (CCC), and stores an instruction address in an address latch, when the instruction related to the address is executed in next clock cycle (NCC) which is associated with CCC, or stores another instruction. The scheduler copies an instruction corresponding to the stored address from cache to an...
...ADVANTAGE - Improves efficiency for processing commercial workloads, as the protocol engine transits from one memory transaction to another in minimum number of clock cycles...

Title Terms.../Index Terms/Additional Words: CLOCK;

Original Publication Data by Authority

Original Abstracts:
...invention relates generally to a protocol engine for use in a multiprocessor computer system. The protocol engine, which implements a cache coherence protocol, includes a clock signal generator for generating signals denoting interleaved even clock periods and odd clock periods, a memory transaction state array for storing entries, each denoting the state of a respective memory transaction, and processing logic. The memory transactions are divided into even and...

...whose states are stored in distinct sets of entries in the memory

transaction state array. The processing logic has interleaving circuitry for processing during even clock periods the even memory transactions and for processing during odd clock periods the odd memory transactions. Moreover, the protocol engine is configured to transition from one memory transaction to another in a minimum number of clock cycles. This design improves efficiency for processing commercial workloads, such as on-line transaction processing (OLTP) by taking certain steps in parallel...

...invention relates generally to a protocol engine for use in a multiprocessor computer system. The protocol engine, which implements a cache coherence protocol, includes a clock signal generator for generating signals denoting interleaved even clock periods and odd clock periods, a memory transaction state array for storing entries, each denoting the state of a respective memory transaction, and processing logic. The memory transactions are divided into even and odd transactions whose states are stored in distinct sets of entries in the memory transaction state array. The processing logic has interleaving circuitry for processing during even clock periods the even memory transactions and for processing during odd clock periods the odd memory transactions. Moreover, the protocol engine is configured to transition from one memory transaction to another in a minimum number of clock cycles. This design improves efficiency for processing commercial workloads, such as on-line transaction processing (OLTP) by taking certain steps in parallel.
Claims:
...implementing a cache coherence protocol, for use in a multiprocessor computer system, the protocol engine comprising:a signal generator configured to generate a series of clock cycles;a memory transaction array configured to store entries representing a plurality of memory transactions, said plurality of memory transactions being associated with the series of clock cycles;execution logic configured to execute during a current clock cycle an instruction corresponding to a memory transaction selected in a previous clock cycle, said memory transaction associated with the current clock cycle; andscheduling logic configured to select during the current clock cycle an active memory transaction associated with the current clock cycle, if any, from among the plurality of memory transactions represented by said entries in said memory transaction array, said scheduling logic configured to then store during the current clock cycle a first instruction address in an instruction address latch when an instruction corresponding to said first instruction address can be executed during a next clock cycle associated with said current clock cycle, said first instruction address corresponding to the memory transaction selected in the previous clock cycle;store during said current clock cycle a second instruction address in said instruction address latch when said instruction corresponding to said first instruction address cannot be executed during said next clock cycle associated with said current clock cycle, said second instruction address corresponding to the active memory transaction; andcopy during a next clock cycle not associated with the current clock cycle an instruction from an instruction cache into an instruction latch, said instruction corresponding to an instruction address stored in said instruction address latch, the execution logic being further configured to execute during said next clock cycle associated with the current clock cycle an instruction stored in the instruction latch.

...

...implementing a cache coherence protocol, for use in a multiprocessor computer system, the protocol engine comprising:a signal generator configured to generate a series of clock cycles;a memory transaction array configured to store entries representing a plurality of memory transactions, said plurality of memory transactions being associated with the series of clock cycles;a message source, said message source including a plurality of message ports and a plurality of input buffers, said plurality of input buffers configured to store messages received through said plurality of message ports;execution logic configured to execute during a current clock cycle an instruction corresponding to a memory transaction scheduled in a previous clock cycle, said memory transaction associated with the current clock cycle; andscheduling logic configured to:identify a plurality of memory transactions, if any, capable of execution during a next clock cycle associated with the current clock cycle, said plurality of memory transactions including one or more of:the memory transaction scheduled in a previous clock cycle;an active memory transaction associated with the current clock cycle stored in the memory transaction array; anda memory transaction corresponding to a message selected from the message source; andschedule during the current clock cycle one of the plurality of memory transactions according to a predefined prioritization scheme.> Basic Derwent Week: 200270

47/3,K/19 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0012447113 - Drawing available
WPI ACC NO: 2002-392705/200242
XRPX Acc No: N2002-307831
Clock data maintaining method used for controlling operation of power machine involves intermittently recording clock data in predetermined clock locations in non-volatile memory
Patent Assignee: BOEN R (BOEN-I); BRANDT K A (BRAN-I); CLARK EQUIPMENT CO (CLAE); FUSS T (FUSS-I); ROSSOW S R (ROSS-I)
Inventor: BOEN R; BRANDT K A; FUSS T; ROSSOW S R
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20020018403	A1	20020214	US 2000221810	P	20000731	200242 B
			US 2001768730	A	20010124	
US 6552965	B2	20030422	US 2001768730	A	20010124	200330 E

Priority Applications (no., kind, date): US 2000221810 P 20000731; US 2001768730 A 20010124

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20020018403	A1	EN	15	8	Related to Provisional US 2000221810

Clock data maintaining method used for controlling operation of power machine involves intermittently recording clock data in predetermined clock locations in non-volatile memory

Original Titles:
Electronic clock

...

...Electronic **clock**

Alerting Abstract ...NOVELTY - The method involves receiving a **clock** signal indicating the elapsed time and intermittently recording the **clock** data in predetermined **clock** locations in a non-volatile memory, such that less number of **clock** locations store the same **clock** data.DESCRIPTION - An INDEPENDENT CLAIM is also included for a **clock** storing time data...

Title Terms/Index Terms/Additional Words: **CLOCK**;

Original Publication Data by Authority

Original Abstracts:
A **clock** stores time data **indicative** of time of operation of a power machine. A timing circuit provides a timing signal and a controller is coupled to a timing circuit and...

...A **clock** stores time data indicative of time of operation **of** a power machine. A timing circuit provides a timing signal and a controller is coupled to a timing circuit and to a memory, which includes...
Claims:
What is claimed is:1. A method of maintaining **clock** data indicative of time of operation of a **power** machine, comprising:providing a plurality of **clock** locations in non-volatile memory;receiving a **clock** signal indicative **of** elapsed time; andintermittently writing **clock** data, indicative of **time** value, to the plurality of **clock** locations such that fewer **than** all of the plurality of an **clock** locations contain **the** same **clock** data at any given time.

What is claimed is:12. A **clock** storing time data indicative of time of operation of a power machine, the **clock** comprising:a timing circuit providing a timing signal;a memory having **a** plurality of time locations; anda controller coupled to the timing circuit and **the** memory, the controller maintains an elapsed time value, based on the timing signal, **and** **selects** a first time location of the plurality of time locations and updates the **selected** first time location **with** the elapsed time value and, after a first update time period, updates a subsequently selected second time location with a first updated elapsed time value. Basic Derwent Week: **200242**

47/3,K/34 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008745014 - Drawing available
WPI ACC NO: 1998-287183/**199825**
XRPX Acc No: N1998-225668
Data cache for performing store cycles in single **clock** cycle - speculatively stores data within predicted way of cache after capturing data currently being stored in same predicted way
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: HATTANGADI R M; WITT D B
Patent Family (5 patents, 85 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update

WO 1998020420 A1 19980514 WO 1996US17517 A 19961104 199825 B
AU 199712708 A 19980529 WO 1996US17517 A 19961104 199841 E
AU 199712708 A 19961104
EP 1015980 A1 20000705 EP 1996943477 A 19961104 200035 E
WO 1996US17517 A 19961104
EP 1015980 B1 20020424 EP 1996943477 A 19961104 200228 E
WO 1996US17517 A 19961104
DE 69620920 E 20020529 DE 69620920 A 19961104 200243 E
EP 1996943477 A 19961104
WO 1996US17517 A 19961104

Priority Applications (no., kind, date): WO 1996US17517 A 19961104

Patent Details
Number Kind Lan Pg Dwg Filing Notes
WO 1998020420 A1 EN 26 4
National Designated States,Original: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN
Regional Designated States,Original: AT BE CH DE DK EA ES FI FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG
AU 199712708 A EN PCT Application WO 1996US17517
Based on OPI patent WO 1998020420
EP 1015980 A1 EN PCT Application WO 1996US17517
Based on OPI patent WO 1998020420
Regional Designated States,Original: DE ES GB
EP 1015980 B1 EN PCT Application WO 1996US17517
Based on OPI patent WO 1998020420
Regional Designated States,Original: DE ES GB
DE 69620920 E DE Application EP 1996943477
PCT Application WO 1996US17517
Based on OPI patent EP 1015980
Based on OPI patent WO 1998020420

Data cache for performing store cycles in single **clock** cycle...

Original Titles:
...A DATA CACHE CAPABLE OF PERFORMING STORE ACCESSES IN A SINGLE **CLOCK** CYCLE...

...A DATA CACHE CAPABLE OF PERFORMING STORE ACCESSES IN A SINGLE **CLOCK** CYCLE...

...A DATA CACHE CAPABLE OF PERFORMING STORE ACCESSES IN A SINGLE **CLOCK** CYCLE

Alerting Abstract ...cache speculatively stores data within a predicted way of the cache after capturing the data currently being stored in that predicted way. During a subsequent **clock** cycle, the cache hit information for the store access validates the way prediction. If the way prediction is correct, then the store is complete. If...

...data cache concurrently with the restoration of data in the predicted storage location. Each store for which the way prediction is correct, uses a single **clock** cycle of data cache bandwidth...

Title Terms.../Index Terms/Additional Words: **CLOCK**;

Original Publication Data by Authority

Original Abstracts:
A data cache configured to perform store accesses in a single clock cycle is provided. The data cache speculatively stores data within a predicted way of the cache after capturing the data currently being stored in that predicted way. During a subsequent clock cycle, the cache hit information for the store access validates the way prediction. If the way prediction is correct, then the store is complete. If the way prediction is...

...data cache concurrently with the restoration of data in the predicted storage location. Each store for which the way prediction is correct utilizes a single clock cycle of data cache bandwidth. Additionally,the way prediction structure implemented within the data cache bypasses the tag comparisons of the data cache to select data bytes for the ...
...A data cache configured to perform store accesses in a single clock cycle is provided. The data cache speculatively stores data within a predicted way of the cache after capturing the data currently being stored in that predicted way. During a subsequent clock cycle, the cache hit information for the store access validates the way prediction. If the way prediction is correct, then the store is complete. If the way prediction is incorrect, then the captured data...

...data cache concurrently with the restoration of data in the predicted storage location. Each store for which the way prediction is correct utilizes a single clock cycle of data cache bandwidth. Additionally,the way prediction structure implemented within the data cache bypasses the tag comparisons of the data cache to select data bytes for the output. Therefore, the access time...
Claims:
...and a data cache control unit (254) coupled to said data array (251), said tag comparison block and said way prediction structure, to cause during a first clock cycle said data array to store said associated input data into said predicted storage location if said input address is associated with a store instruction, said input data being stored prior to determining if said predicted storage location is storing data associated with said input address but after reading out said n output data in said n-to-one way selection device; characterised by: a register (259) coupled to said n-to- one way selection device (257) and configured to receive and store said data selected by the n-to-one way selection device in said first clock cycle and to provide said predicted storage location in said data array (251) with said stored data for restoration in the next clock cycle; a data selection device (260) coupled to said data array (251) and to said data cache control unit (254) which receives hit predicted way and hit inpredicted way signals (263, 264) from said tag comparison block, said selection device configured to receive said input data and said data provided by said register (259) such that, during said next clock cycle, the data selection device (260) selectively provides to a second data input port of said data array (251) either a) said data...
...262) determining either that none of said indexed storage locations is storing data associated with said input address or that the data is stored in a storage location not predicted (264) by the way prediction structure (255, 268), or b) input data on said input data bus (253) in response to...

...with said input address is the storage location predicted (263) by the way prediction structure (255, 268); and wherein, if said tag comparison block (262) determines in said next clock cycle that said

input data is stored in a location not predicted by the way prediction structure, the cache control unit (254) again accesses at the first data input port the indexed plurality of storage locations **accessed** in the first clock cycle and the data associated with the input address is thereby stored in the storage location determined by the tag **comparison** block (262) which provides the data array (251) with the correct way of data cache (267) for said store access of said input address.

...
...

47/3,K/35 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008702568 - Drawing available
WPI ACC NO: 1998-242813/**199822**
XRPX Acc No: N1998-192137
Interpolation circuit for encoder, especially interpolation circuit for digital interpolation processing - has phase angle data detecting circuit which detects and stores phase angle data for each first **clock**, which is input to updating circuit
Patent Assignee: MITUTOYO CORP (MIUT); MITUTOYO KK (MIUT)
Inventor: KIRIYAMA T; TERAGUCHI M
Patent Family (8 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 840096	A1	19980506	EP 1997117951	A	19971016	199822 B
JP 10132606	A	19980522	JP 1996286847	A	19961029	199831 E
US 5907298	A	19990525	US 1997949620	A	19971014	199928 E
JP 3015747	B2	20000306	JP 1996286847	A	19961029	200016 E
EP 840096	B1	20010321	EP 1997117951	A	19971016	200117 E
DE 69704323	E	20010426	DE 69704323	A	19971016	200130 E
			EP 1997117951	A	19971016	
CN 1182979	A	19980527	CN 1997122411	A	19971029	200242 E
CN 1103139	C	20030312	CN 1997122411	A	19971029	200537 E

Priority Applications (no., kind, date): JP 1996286847 A 19961029

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 840096	A1	EN	22	14	

Regional Designated States,Original: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

JP 10132606	A	JA	10	
JP 3015747	B2	JA	10	Previously issued patent JP 10132606

EP 840096	B1	EN	

Regional Designated States,Original: DE GB

DE 69704323	E	DE	Application EP 1997117951
			Based on OPI patent EP 840096

...has phase angle data detecting circuit which detects and stores phase angle data for each first **clock**, which is input to updating circuit

Alerting Abstract ...The interpolation circuit includes **clock** generator which generates two synchronised **clock** signals, with the second **clock** having a higher frequency, a phase angle detecting circuit which samples two-phase sinusoidal signals output from the encoder with 90(deg) phase-shift of each other by the first **clock**, and then

digital-processes the resultant sampled values to detect phase angle of the two-phase sinusoidal signals so as to **sequentially** output phase angle data, each corresponding to the respective sampling phase defined by the first **clock**. A data updating circuit **sequentially** inputs the phase angle data from the phase angle detecting circuit, updates the current phase angle data by subsequent phase angle data in such a...

...current and subsequent phase angle data, and then adds the differential data, with the upper limit predetermined, to the current phase angle data, thereby holding **sequentially** updated phase angle data...

...An integrating circuit integrates the differential data by the second **clock** to hold the integrated value which is to be reset by the first **clock**. A carry detecting circuit detects that the integrated value is over the ratio of the first **clock** period to the second **clock** period to output a carry detecting signal, and...

...a two-phase square wave generating circuit generates two-phase square wave, state of which **changes** synchronously with the **second clock** at each timing of the carry detecting signal. The phase angle detecting circuit comprises a sample-and-hold circuit which samples the two-phase sinusoidal signals by the first **clock** and holds the sampled values, AD converter which converts the sampled values to a set of digital data, look-up table memory which outputs a phase angle data based on the set of digital data, and first data storing circuit which **sequentially** stores the phase angle data read out from the look-up table memory synchronously with the first **clock**.

Title Terms.../Index Terms/Additional Words: **CLOCK**;

Original Publication Data by Authority

Original Abstracts:
...accuracy is improved is disclosed. The phase angle data detecting circuit 1 detects to store the phase angle data PH for each of the first **clock** CK1. The phase **angle** data PH is input to the updating circuit 2 in which the current data CNT is subtracted from the subsequent phase angle data PH so...

...to be added to the current data CNT. The integrating circuit 3 integrates the differential data DELTA1, whose upper limit is predetermined, by the second **clock** CK2 to generate **the** carry signal QUADEN at each timing when the integrated value leads to the period ratio of CK1 to CK2. The two-phase square wave generating...

...An interpolation circuit of an encoder of which dynamic accuracy is improved is disclosed. The phase angle data detecting circuit 1 detects to **store** the phase angle data PH for each of **the** first **clock** CK1. The phase angle data PH is input **to** the **updating circuit** 2 in which the current data CNT **is** subtracted from the subsequent phase angle data PH so as to be **updated**. The differential data DX is limited within an **upper** limit to be added to the current data CNT. The integrating circuit 3 integrates the differential data DELTA1, whose upper limit is predetermined, by the second **clock** CK2 to generate the carry signal QUADEN at **each** timing when the integrated value leads to the period ratio of CK1 to CK2. The two-phase square wave generating circuit 5 generates two-phase...
Claims:
1. An interpolation circuit for an encoder, comprising:</br> a **clock**

generator which generates a first clock and a second clock, the second clock being synchronized with the first clock and having a higher frequency than the first clock;</br> a phase angle detecting circuit which samples two-phase sinusoidal signals output from the encoder with 90(deg) phase-shift each other by the first clock, and then digital-processes the resultant sampled values to detect phase angle of the two-phase sinusoidal signals so as to sequentially output phase angle data, each phase angle data corresponding to the respective sampling phase defined by the first clock;</br> a data updating circuit which sequentially input the phase angle data output from the phase angle detecting circuit, and then updates the current phase angle data by the subsequent phase angle data in such a manner as to calculate...

...and the subsequent phase angle data, and then adds the differential data, whose upper limit is predetermined, to the current phase angle data, thereby holding sequentially updated phase angle data;</br> an integrating circuit which integrates the differential data by the second clock to hold the integrated value which is to be reset by the first clock;</br> a carry detecting circuit which detects that the integrated value is over the ratio of the first clock period to the second clock period to output a carry detecting signal; and</br> a two-phase square wave generating circuit which generates two-phase square wave, state of which changes synchronously with the second clock at each timing of the carry detecting signal.

...

...An interpolation circuit for an encoder, comprising:a clock generator (7) which generates a first clock (CK1);a phase angle detecting circuit (1) which samples two-phase sinusoidal signals output from the encoder with 90(deg) phase shift to each other by the first clock, and then digital-processes the resultant sampled values to detect a phase angle of the two-phase sinusoidal signals so as to sequentially output phase angle data, each phase angle data corresponding to the respective sampling phase defined by the first clock (CK1);a data updating circuit (2) which sequentially inputs the phase angle data output from the phase angle detecting circuit, and then updates the current phase angle data by the subsequent phase angle data in such a manner as to calculate a differential between the current phase angle data and the subsequent phase angle data, and then adds the differential data, whose upper limit is predetermined, to the current phase angle data, thereby holding sequentially updated phase angle data; andan integrating circuit (3),characterized in thatsaid clock generator (7) is adapted for generating a second clock (CK2), the second clock (CK2) being synchronized with the first clock (CK1) and having a higher frequency than the first clock (CK1);said integrating circuit (3) is adapted for integrating the differential data by the second clock (CK2) to hold the integrated value which is to be reset by the first clock (CK1);a carry detecting circuit (4) which detects that the integrated value is over the ratio of the first clock period to the second clock period to output a carry detecting signal; anda two-phase square wave generating circuit (5) which generates two-phase square wave signals, the state of which changes synchronously with the second clock (CK2) at each timing of the carry detecting signal....
Basic Derwent Week: 199822...

47/3,K/42 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007898100 - Drawing available
WPI ACC NO: 1996-211338/199622
XRPX Acc No: N1996-176830
Digital signal recording apparatus e.g. VCR - generates parallel bit channel words at slower rate than system clock using inverting precoders and performs decision procedure
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM S; KIM S T
Patent Family (18 patents, 13 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 709845	A2	19960501	EP 1995307729	A	19951030	199622 B
TW 274137	A	19960411	TW 1995110891	A	19951017	199629 E
CA 2161609	A	19960501	CA 2161609	A	19951027	199635 E
JP 8255433	A	19961001	JP 1995282277	A	19951030	199649 E
BR 199504306	A	19970408	BR 19954306	A	19951005	199720 E
US 5745312	A	19980428	US 1995472275	A	19950607	199824 E
			US 1997800131	A	19970213	
US 5877712	A	19990302	US 1995472275	A	19950607	199916 E
			US 1995506041	A	19950724	
			US 1997868830	A	19970609	
KR 160732	B1	19990115	KR 199539052	A	19951031	200036 E
RU 2150149	C1	20000527	RU 1995118718	A	19951030	200057 E
CN 1144378	A	19970305	CN 1995118541	A	19951030	200064 E
EP 709845	B1	20011219	EP 1995307729	A	19951030	200206 E
MX 198535	B	20000912	MX 19954569	A	19951030	200211 E
CA 2161609	C	20020205	CA 2161609	A	19951027	200213 E
DE 69524712	E	20020131	DE 69524712	A	19951030	200216 E
			EP 1995307729	A	19951030	
US 6384996	B1	20020507	US 1995472275	A	19950607	200235 E
ES 2167406	T3	20020516	EP 1995307729	A	19951030	200239 E
US 20020105745	A1	20020808	US 1995472275	A	19950607	200254 E
			US 2002108411	A	20020329	
CN 1080919	C	20020313	CN 1995118541	A	19951030	200516 E

Priority Applications (no., kind, date): EP 1995307729 A 19951030; KR 199428377 A 19941031

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 709845	A2	EN	49	19	
Regional Designated States,Original: DE ES FR GB NL					
TW 274137	A	ZH			
CA 2161609	A	EN			
JP 8255433	A	JA	33		
BR 199504306	A	PT			
US 5745312	A	EN	30		Division of application US 1995472275
US 5877712	A	EN			C-I-P of application US 1995472275
					C-I-P of application US 1995506041
					C-I-P of patent US 5642241
EP 709845	B1	EN			
Regional Designated States,Original: DE ES FR GB NL					
CA 2161609	C	EN			
DE 69524712	E	DE			Application EP 1995307729
					Based on OPI patent EP 709845
ES 2167406	T3	ES			Application EP 1995307729

Based on OPI patent EP 709845
US 20020105745 A1 EN Division of application US 1995472275

Division of patent US 6384996

...generates parallel bit channel words at slower rate than system **clock** using inverting precoders and performs decision procedure
Original Titles:
...Calculating, at rate faster than I-NRZI modulation **clock** rate, ones and zeroes for insertion into I-NRZI modulation...

Alerting Abstract ...recording apparatus includes a recorder, an input port, circuitry for inserting a zero or a one into information words, two precoders, a selector, a selector **switch** and **two** parallel to **serial converters**. The precoders convert positive words to negative words, and negative to positive. The selector chooses a pair of positive and negative information words...

Title Terms.../Index Terms/Additional Words: **CLOCK**;

Original Publication Data by Authority

Original Abstracts:
...the channel words that are selected between for recording. The precoders (106) perform precoding on an accelerated basis using ripple-through integration of the alternate **successive** bits used to **form** each channel word. Two precoders (106) generate (n+1)-parallel-bit channel words at a channel word rate slower by a factor of (n+1) than the rate of a system **clock** for the I-**NRZI** modulation. This leaves additional time during each channel word interval to carry out a decision procedure, which determines which of the channel words generated by the two precoders is to be selected for recording. There is also sufficient additional time for completing a subsequent **updating** procedure,in which **precoding** information **stored** in the precoder **that** did not generate the selected channel word is altered, to conform to precoding information **stored** in the precoder **that** did generate the selected channel word. The parallel-bit channel words from the precoders (106) are converted to **serial**-bit format for **recording** with a bit rate equal to that **of** the system **clock**. The parallel-bit **channel** words from the precoders are converted to **serial**-bit format with **an** effective bit rate that is substantially higher than that of the system **clock**, to provide a **signal** for timely implementing the decision and **updating** procedures.

...

...generate the channel words that are selected between for recording. The precoders perform preceding on an accelerated basis using ripple-through integration of the alternate **successive** bits used to form each channel word. Two **precoders** generate (n+1)-parallel-bit channel words at a channel word rate slower by a factor of (n+1) than the rate of a system **clock** for the I-NRZI modulation. This leaves additional **time** during each channel word interval to carry out a decision procedure, which determines which of the channel words generated by the two precoders is to be selected for recording. There is also sufficient additional time for completing a subsequent **updating** procedure, in which preceding information **stored** in the **precoder** that did not generate the **selected** channel word is altered, to conform to preceding information **stored** in the precoder that did generate the selected **channel** word. The parallel-bit channel words from the

precoders are converted to serial-bit format for recording with a bit rate equal to that of the system clock. The parallel-bit channel words from the precoders are converted to serial-bit format with an effective bit rate that is substantially higher than that of the system clock, to provide signal for timely implementing the decision and updating procedures.

...

...generate the channel words that are selected between for recording. The precoders perform preceding on an accelerated basis using ripple-through integration of the alternate successive bits used to form each channel word. Two precoders generate (n+1)-parallel-bit channel words at a channel word rate slower by a factor of (n+1) than the rate of a system clock for the I-NRZI modulation. This leaves additional time during each channel word interval to carry out a decision procedure, which determines which of the channel words generated by the two precoders is to be selected for recording. There is also sufficient additional time for completing a subsequent updating procedure, in which preceding information stored in the precoder that did not generate the selected channel word is altered, to conform to precoding information stored in the precoder that did generate the selected channel word. The parallel-bit channel words from the precoders are converted to serial-bit format for recording with a bit rate equal to that of the system clock. The parallel-bit channel words from the precoders are converted to serial-bit format with an effective bit rate that is substantially higher than that of the system clock, to provide signal for timely implementing the decision and updating procedures.

...

...generate the channel words that are selected between for recording. The precoders perform preceding on an accelerated basis using ripple-through integration of the alternate successive bits used to form each channel word. Two precoders generate (n+1)-parallel-bit channel words at a channel word rate slower by a factor of (n+1) than the rate of a system clock for the I-NRZI modulation. This leaves additional time during each channel word interval to carry out a decision procedure, which determines which of the channel words generated by the two precoders is to be selected for recording. There is also sufficient additional time for completing a subsequent updating procedure, in which preceding information stored in the precoder that did not generate the selected channel word is altered, to conform to preceding information stored in the precoder that did generate the selected channel word. The parallel-bit channel words from the precoders are converted to serial-bit format for recording with a bit rate equal to that of the system clock. The parallel-bit channel words from the precoders are converted to serial-bit format with an effective bit rate that is substantially higher than that of the system clock, to provide signal for timely implementing the decision and updating procedures.

...

...generate the channel words that are selected between for recording. The precoders perform preceding on an accelerated basis using ripple-through integration of the alternate successive bits used to form each channel word. Two precoders generate (n+1)-parallel-bit channel words at a channel word rate slower by a factor of (n+1) than the rate of a system clock for the I-NRZI modulation. This leaves additional time

during each channel word interval to carry out a decision **procedure**, which determines which of the channel words generated by the two precoders is to be selected for recording. There is also sufficient additional time for completing a subsequent **updating** procedure, in which precoding information **stored** in the precoder that did not generate the selected channel word is altered, **to** conform to preceding information **stored in** the precoder that did generate the selected channel word. The parallel-bit channel words from the precoders are **converted** to **serial**-bit format for recording with a bit rate equal to that of the system clock. The parallel-bit channel **words** from the precoders are converted to **serial**-bit format with an effective bit **rate that** is substantially higher than that of the system **clock**, to provide **signal** for timely implementing the decision and **updating** procedures.
Claims:
...Digital signal recording apparatus comprising: a recorder (120), for recording parallel tracks of digital signal modulation on a recording medium; an input port (101) for **serially** receiving n-bit **information** words; circuitry (104.1) for inserting a "0" bit into each said received n-bit information word and generating a (n+1)-parallel-bit "positive" information word at an information word rate slower by a factor of (n+1) than the rate of a system **clock**; circuitry (104.2) for **inserting** a "1" bit into each said received n-bit information word and generating a (n+1)-parallel-bit "negative" information word at said information word...

...n+1)-parallel-bit channel word, generated at a channel word rate slower by a factor of (n+1) than the rate of said system **clock**; a second precoder (106.2) for **coding** each (n+1)-parallel-bit "**positive**" information word to **convert** it into a corresponding "negative"-information (n+1)-parallel-bit channel word, generated at said channel word rate; means (108, 110, 112, 114, 116, 118) for selecting one of each concurrent pair of "positive"-information and "negative"-information (n+1)-parallel-bit channel words for **serial** recording at said system **clock** rate, said means **for** selecting one of each **concurrent** pair of (n+1)-parallel-bit channel words for recording including a selector switch (118) responsive to a control signal to select signal for application to said recorder in **serial** -bit form at said system **clock** rate, and first **parallel**-to-**serial** conversion means (108) **for** generating first parallel-to-**serial** conversion **results** by converting to **serial**-bit form the (n+1)-parallel-bit channel word selected **by** said selector switch (118), for **serial** recording at said system **clock** rate; **second parallel**-to-**serial** **conversion** means (110) for generating **second** parallel-to-**serial** conversion results **by converting** at least one of each concurrent pair **of** (n+1)-parallel-bit channel words to **serial**-bit form; and a control signal generator (116) for selecting a **prescribed** spectral response for the one of the parallel tracks on said magnetic recording medium being currently recorded, for determining from said second parallel-to-**serial** conversion results how much respective spectral responses for "positive"-information and "negative"-**information** (n+1)-parallel-bit channel words most recently generated by said first and second precoders will deviate in energy from said prescribed spectral response if...Digital signal recording apparatus comprising: a recorder (120), for recording parallel tracks of digital signal modulation on a recording medium; an input port (101) for **serially** receiving n-bit information words; circuitry (104.1) for inserting a "0" bit into each said received n-bit information word and generating a (n...

...1" bit into each said received n-bit information word and generating a (n+1)-parallel-bit second information word, which (n+1)-parallel-bit second information word is supplied concurrently with said (n+1)-parallel-bit first information word generated from the same one of said n-bit information words; a first precoder (106.1) for coding each (n+1)-parallel-bit first information word to convert it into a corresponding first-information (n+1)-parallel-bit channel word; a second precoder (106.2) for coding each (n+1)-parallel-bit second information word to convert it into a corresponding second-information (n+1)-parallel-bit channel word; a control signal generator (116) for analysing frequency characteristics of the (n+1...

...desired frequency characteristic on the basis of the analysed spectrum; characterised in that: said circuitry (104.1) for inserting a "0" bit into each said received n-bit information word and generating a (n+1)-parallel-bit first information word does so at an information word rate slower by a factor of (n+1) than the rate of a system clock; said circuitry (104.2) for inserting a "1" bit into each said received n-bit information word and generating a (n+1)-parallel-bit second ...

...it into a corresponding first-information (n+1)-parallel-bit channel word, generates at a channel word rate slower by a factor of (n+1) than the rate of said system clock; said second precoder (106.2) for coding each (n+1)-parallel-bit first information word to convert it into a corresponding second-information (n+1)-parallel-bit channel word, generates at said channel word rate; and the apparatus further comprises: means (108, 110, 112, 114, 116, 118) for selecting one of each concurrent pair of first-information and second-information (n+1)-parallel-bit channel words for serial recording at said system clock rate, said means for selecting one of each concurrent pair of (n+1)-parallel-bit channel words for recording including a selector switch (118) responsive to a control signal to select a signal for application to said recorder in serial-bit form at said system clock rate, and first parallel-to-serial conversion means (108) for generating first parallel-to-serial conversion results by converting to serial-bit form the (n+1)-parallel-bit channel word selected by said selector switch (118), for serial recording at said system clock rate; second parallel-to-serial conversion means (110) for generating second parallel-to-serial conversion results by converting at least one of each concurrent pair of (n+1)-parallel-bit channel words to serial-bit form; and said control signal generator (116) for selecting a prescribed spectral response for the one of the parallel tracks on said magnetic recording medium being currently recorded, for determining from said second parallel-to-serial conversion results how much respective spectral responses for first-information and second-information (n+1)-parallel-bit channel words most recently generated by said first and second precoders will deviate in energy from said prescribed spectral response if recorded in a prescribed non-return-to-zero-invert-on-ONEs format, and for comparing the amplitudes of the respective deviation results for the first-information ...n+1)-parallel-bit channel words most recently generated by said first and second precoders (106.1, 106.2), to generate a control signal indicating which one of said first-information and second-information (n+1)-bit channel words has a spectral response that least deviates from said prescribed spectral response....is: 1. Digital signal recording apparatus comprising: a recorder, for recording parallel tracks of digital signal modulation on a recording medium; an input port for serially receiving n-bit information words; circuitry for inserting a

"0" bit into each said received n-bit information word and generating a (n+1)-parallel-bit "positive" information word at an information word rate slower by a factor of (n+1) than the rate of a system **clock**; circuitry for inserting a "1" bit into each said received n-bit information word and generating a (n+1)-parallel-bit "negative" information word at...

...into a corresponding "positive"-information (n+1)-parallel-bit channel word, generated at a channel word rate slower by a factor of (n+1) than **the** rate of said system **clock**; a second precoder for coding each (n+1)-parallel-bit "negative" information word to convert it into a corresponding "negative"-information (n+1)-parallel-bit channel word, generated at said channel word rate; means for selecting one of each concurrent pair of "positive"-information **and** "negative"-information (n+1)-parallel-bit channel words for **serial** recording at said system **clock** rate, said means for selecting one of each concurrent pair of (n+1)-parallel-bit channel words for recording including a selector switch responsive to a control signal to select signal for application to said recorder in **serial**-bit form at said system **clock** rate, and first parallel-to-**serial** conversion means for generating first parallel-to-**serial** conversion results by converting to **serial** -bit form the (n+1)-parallel-bit channel word selected by said selector switch, for **serial** recording at said system **clock** rate; second parallel-to-**serial** conversion means for generating second **parallel**-to-**serial** conversion **results** by **converting** at least one of each concurrent pair of (n+1)parallel-bit channel words to **serial**-bit form; and a control signal generator for selecting a prescribed spectral response for the one of the parallel tracks on said magnetic recording medium being currently recorded, for determining from said second parallel-to-**serial** **conversion** results how much respective **spectral** responses for "positive"-information and "negative"-information (n+1)-parallel-bit channel words most recently generated by said first and **second** precoders will deviate **in** energy from said prescribed spectral response if recorded in a prescribed non-return-to-**zero**-invert-on-ONEs format, and **for** comparing the amplitudes of the respective deviation **results** for the "positive"-information and "negative"-information (**n**+1)-parallel-bit channel words **most** recently generated by said first and second precoders, to generate a control signal indicating which **one** of said "positive"-information **and** "negative"-information (n+1)-bit channel words has **a** spectral response that least deviates from said **prescribed** spectral response.

Digital signal recording apparatus comprising: **a** recorder, for recording parallel tracks of digital signal modulation on a recording medium; an input port for **serially** receiving n-bit information words; circuitry for inserting a "0" bit into each said received n-bit information word and generating a (n+1)-parallel-bit "positive"information word at an information word rate slower by a factor of (n+1) than the rate of a system **clock**; circuitry for inserting a "1" bit into each said received n-bit information word and generating a (n+1)-parallel-bit "negative" information word at...

...n+1)-parallel-bit channel word, generated at a channel word rate slower by a factor of (n+1) than the rate of said system **clock**; a second precoder for coding each (n+1)-parallel-bit "negative" information word to convert it into a corresponding "negative"-information (n+1)-parallel-**bit** channel word, generated at said channel word rate; means for selecting one of each concurrent pair of "positive"-information and "negative"-information (n+1)-parallel-bit channel words for **serial** recording at said system **clock** rate, said means for selecting one of each concurrent pair of (n+1)-parallel-**bit** channel words for

recording including first parallel-to-serial conversion means for generating first parallel-to-serial conversion results by converting the selected (n+1)-parallel-bit channel word to serial-bit form, and a selector switch responsive to a control signal for selecting one of said first parallel-to-serial conversion results for application to said recorder, for serial recording at said system clock rate; second parallel-to-serial conversion means for generating second parallel-to-serial conversion results by converting at least one of each concurrent pair of (n+1)-parallel-bit channel words to serial-bit form; and li> a control signal generator for selecting a prescribed spectral response for the one of the parallel tracks on said magnetic recording medium being currently recorded, for determining from said second parallel-to-serial conversion results how much respective spectral responses for "positive"-information and "negative"-information (n+1)-parallel-bit channel words most recently generated by said first and second precoders will deviate in energy from said prescribed spectral response if recorded in a prescribed non-return-to-zero-invert-on-ONEs format, and for comparing the amplitudes of the respective deviation results for the "positive"-information and "negative"-information (n+1)-parallel-bit channel words most recently generated by said first and second precoders, to generate a control signal indicating which one of said "positive"-information and "negative"-information (n+1)-bit channel words has a spectral response that least deviates from said prescribed spectral response, wherein said second parallel-to-serial conversion means converts said "positive"-information and "negative"-information (n+1)-parallel-bit channel words to respective (n+1)-serial-bit channel words, each of which is supplied to said control signal generator at a second clock rate that is substantially higher than said system clock rate.

A 2T precoder for a succession of digital words including a current digital word, each of said digital words having a bit length (M-1) where M is a positive...

...temporarily store a particular bit insertion value and further including respective second through Mthbit latches to receive and temporarily store the first through (M-1)th consecutive bits of said current digital word; and first through Mth two-input exclusive-OR gates connected to receive as respective first inputs the bits respectively stored in said first through Mth bit latches of said M-parallel-bit-out register, said third through Mth exclusive-OR gates connected to receive as respective second inputs the first through (M-2)th consecutive bits of an M-bit current channel word, said first and second exclusive-OR gates connected to receive as respective second inputs the penultimate and last consecutive bits of an immediately previous channel word, said first through Mth exclusive-OR gates supplying respective responses for defining the consecutive bits of said M-bit current channel word and providing a serial-word, parallel-bits-per-word 2T precoding result as soon as ripple propagation through said first through Mth exclusive-OR gates is completed ...

...Digital signal recording apparatus comprising: a recorder, for recording parallel tracks of digital signal modulation on a recording medium; an input port for serially receiving n-bit information words; circuitry for inserting a "0" bit into each said received n-bit information word and generating a (n+1)-parallel-bit "positive" information word at an information word rate slower by a factor of (n+1) than the rate of a system clock; circuitry for inserting a "1" bit into each said received n-bit information word and generating a (n+1)-parallel-bit

"negative" information word at said information word rate, which (n+1)-parallel-bit "negative" information word is supplied concurrently with said (n+1)-parallel-bit "positive" information word generated from the same one of said n-bit information words; a first precoder for coding each (n+1)-parallel-bit "positive" information word to convert it into a corresponding "positive"-information (n+1)-parallel-bit channel word, generated at a channel word rate slower by a factor of (n+1) than the rate of said system clock; a second precoder for coding each (n+1)-parallel-bit "negative" information word to convert it into a corresponding "negative"-information (n+1)-parallel...

...at said channel word rate; means for selecting one of each concurrent pair of "positive"-information and "negative"-information (n+1)-parallel-bit channel words for serial recording at said system clock rate, said means for selecting one of each concurrent pair of (n+1)-parallel-bit channel words for recording including first parallel-to-serial conversion means for generating first parallel-to-serial conversion results by converting the selected (n+1)-parallel-bit channel word to serial-bit form, and a selector switch responsive to a control signal for selecting one of said first parallel-to-serial conversion results for application to said recorder, for serial recording at said system clock rate; second parallel-to-serial conversion means for generating second parallel-to-serial conversion results by converting at least one of each concurrent pair of (n+1)-parallel-bit channel words to serial-bit form; and a control signal generator for selecting a prescribed spectral response for the one of the parallel tracks on said magnetic recording medium being currently recorded, for determining from said second parallel-to-serial conversion results how much respective spectral responses for "positive"-information and "negative"-information (n+1)-parallel-bit channel words most recently generated by said first and second precoders will deviate in energy from said prescribed spectral response if recorded i...on-ONEs format, and for comparing the amplitudes of the respective deviation results for the "positive"-information and "negative"-information (n+1)-parallel-bit channel words most recently generated by said first and second precoders, to generate a control signal indicating which one of said "positive"-information and "negative"-information (n+1)-bit channel words has a spectral response that least deviates from said prescribed spectral response.

...

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47/3,K/47 (Item 33 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007612506 - Drawing available
WPI ACC NO: 1996-230137/199623
Related WPI Acc No: 1997-457023
XRPX Acc No: N1996-193267
Integrated circuit memory device with two banks of NAND structured memory cells - has clock input for synchronously latching control, address and data signals, with time delays of sequentially accessing and restoring memory bits being masked by dual bank architecture
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: ZAGAR P
Patent Family (10 patents, 65 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 5513148	A	19960430	US 1994348552	A	19941201	199623 B

WO 1996017355 A1 19960606 WO 1995US15558 A 19951130 199628 E
AU 199642902 A 19960619 AU 199642902 A 19951130 199640 E
EP 744073 A1 19961127 EP 1995941501 A 19951130 199701 E
WO 1995US15558 A 19951130
JP 9507948 W 19970812 WO 1995US15558 A 19951130 199742 E
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KR 1997700915 A 19970212 WO 1995US15558 A 19951130 199809 E
KR 1996704093 A 19960729
KR 206063 B1 19990701 WO 1995US15558 A 19951130 200063 E
KR 1996704093 A 19960729
EP 744073 B1 20020417 EP 1995941501 A 19951130 200227 E
WO 1995US15558 A 19951130
EP 2001123861 A 19951130
EP 1191538 A1 20020327 EP 1995941501 A 19951130 200229 E
EP 2001123861 A 19951130
DE 69526431 E 20020523 DE 69526431 A 19951130 200241 E
EP 1995941501 A 19951130
WO 1995US15558 A 19951130

Priority Applications (no., kind, date): US 1994348552 A 19941201

Patent Details
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US 5513148 A EN 11 6
WO 1996017355 A1 EN 26 6
National Designated States,Original: AL AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TT UA UG UZ VN
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG
AU 199642902 A EN Based on OPI patent WO 1996017355
EP 744073 A1 EN 1 PCT Application WO 1995US15558
Based on OPI patent WO 1996017355
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE
JP 9507948 W JA 25 PCT Application WO 1995US15558
Based on OPI patent WO 1996017355
KR 1997700915 A KO PCT Application WO 1995US15558
Based on OPI patent WO 1996017355
KR 206063 B1 KO PCT Application WO 1995US15558
EP 744073 B1 EN PCT Application WO 1995US15558
Related to application EP 2001123861
Related to patent EP 1191538
Based on OPI patent WO 1996017355
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LI LT LU LV MC NL PT SE SI
EP 1191538 A1 EN Division of application EP 1995941501

Division of patent EP 744073
Regional Designated States,Original: AT BE CH DE DK ES FR GB GR IE IT LI LT LU LV MC NL PT SE SI
DE 69526431 E DE Application EP 1995941501
PCT Application WO 1995US15558
Based on OPI patent EP 744073
Based on OPI patent WO 1996017355

...has **clock** input for synchronously latching control, address and data signals, with time delays of sequentially accessing and restoring memory bits being masked by dual bank architecture

Alerting Abstract ...The integrated circuit memory device has a

clock node for receiving a clock signal, and a number of latches connected to the clock node for latching address signals, data signals and control signals into the memory in synchronisation with the clock signal. A data latch is connected to the clock node and to an output node of the memory for latching an output signal to the output node w.r.t. the control signals and in synchronisation with the clock signal...

...A word line activation circuit is connected to the number of word lines, and responds to the control signals and the address signals for activating the word lines in a sequence. A NAND structured memory cell is connected to the number of word lines and to a bit line. A sense amplifier is connected to the bit line, and a...

Title Terms.../Index Terms/Additional Words: CLOCK;

Original Publication Data by Authority

Original Abstracts:
An integrated circuit memory device has two banks of NAND structured memory cells and a clock input for synchronously latching control, address and data signals. Time delays of sequentially accessing and restoring memory bits in the NAND structure are masked through the use of the dual bank architecture and synchronous timing. The NAND structured memory cells provide an extremely dense memory array for a high capacity memory device. The input clock signal driving a synchronous word line generator provides a simplified high speed access to the array. A set of random access storage registers temporarily store data from the array...

...An integrated circuit memory device has two banks of NAND structured memory cells and a clock input for synchronously latching control, address and data signals. Time delays of sequentially accessing and restoring memory bits in the NAND structure are masked through the use of the dual bank architecture and synchronous timing. The NAND structured memory cells provide an extremely dense memory array for a high capacity memory device. The input clock signal driving a synchronous word line generator provides a simplified high speed access to the array. A set of random access storage registers temporarily store data from the array and provide high speed page...

...An integrated circuit memory device has two banks of NAND structured memory cells and a clock input for synchronously latching control, address and data signals. Time delays of sequentially accessing and restoring memory bits in the NAND structure are masked through the use of the dual bank architecture and synchronous timing. The NAND structured memory cells provide an extremely dense memory array for a high capacity memory device. The input clock signal driving a synchronous word line generator provides a simplified high speed access to the array. A set of random access storage registers temporarily store data from the array and provide high speed page access to an entire page...

...An integrated circuit memory device has two banks of NAND structured memory cells and a clock input for synchronously latching control, address and data signals. Time delays of sequentially accessing and restoring memory bits in the NAND structure are masked through the use of the dual bank architecture and synchronous timing. The NAND structured memory cells provide an extremely dense memory array for a high capacity memory device. The input clock signal driving a synchronous word line generator provides a simplified high speed access to the array. A

set of random access storage registers temporarily store data from the array and provide high speed page access to an entire page of data from each bank...
Claims:
...high speed access of data within a memory device having first and second banks of NAND structured memory cells and input nodes for receiving a clock signal, control signals and address signals, the method comprising: a) activating a first series of word lines of the first bank of NAND structured memory cells; b) accessing a first data word from the first bank of NAND structured memory cells in response to the clock, control and address signals; c) advancing an address counter; d) accessing a second data word from the first bank of NAND structured memory cells; e) activating a second series of word lines of the second bank of NAND structured memory cells while data from the first bank of NAND structured memory cells is being accessed; and f) accessing a third data word from the second bank of NAND structured memory cells in response to the clock, control and address signals.

The integrated circuit memory device has a clock node for receiving a clock signal, and a number of latches connected to the clock node for latching address signals, data signals and control signals into the memory in synchronisation with the clock signal. A data latch is connected to the clock node and to an output node of the memory for latching an output signal to the output node w.r.t. the control signals and in synchronisation with the clock signal.

...

...A word line activation circuit is connected to the number of word lines, and responds to the control signals and the address signals for activating the word lines in a sequence. A NAND structured memory cell is connected to the number of word lines and to a bit line. A sense amplifier is connected to the bit line, and a number of random access storage registers are connected to the sense amplifier and to the data latch. The...

...An integrated circuit memory device comprising: a) a clock node (10) for receiving a clock signal; b) a plurality of latches (50-80) connected to said clock node for latching address signals, data signals and control signals into the memory device in synchronization with the clock signal; c) a data latch (70) connected to said clock node and to an output node of the memory device for latching an output signal to the output node in response to the control signals and in synchronization with the clock signal; d) a plurality of word lines (120-126); e) a word line activation circuit (110) connected to said plurality of word lines, the word line activation circuit comprises a mechanism for activating and deactivating a succession of said plurality of word lines in response to said address signals and said control signals (40), said succession of said plurality of word lines being activated and deactivated in synchronization with the clock signal; f) a first bank of NAND structured memory cells (140-146) connected to said plurality of word lines and to a bit line; g) a sense amplifier (154) connected to the bit line; and characterized by further comprising h) a first plurality of random access storage registers (156) connected to said sense amplifier and to said data ...An integrated circuit memory device comprising: a) a clock node for receiving a clock signal; b) a plurality of latches connected to said clock node for latching address signals, data signals and control signals into

the memory device in synchronization with the clock signal; c) a data latch connected to said clock node and to an output node of the memory device for latching an output signal to the output node in response to the control signals and in synchronization with the clock signal; d) a plurality of word lines; e) a word line activation circuit connected to said plurality of word lines, responsive to the control signals and the address signals for activating said plurality of word lines in a sequence; f) a NAND structured memory cell connected to said plurality of word lines and to a bit line; g) a sense amplifier connected to the bit line; and h) a plurality of random access storage registers connected to said sense amplifier and to said data latch. ...
...

47/3,K/48 (Item 34 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007565759 - Drawing available
WPI ACC NO: 1996-181246/199619
XRPX Acc No: N1996-152285
Array clocking system for input-output subsystems - uses clock positioning circuit to position in time, signals generated from system clock and combined with other clock signals to generate single clock
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: ARIMILLI R K; DODSON J S; LEWIS J D
Patent Family (4 patents, 6 countries)

Patent		Application				
Number	Kind	Date	Number	Kind	Date	Update
EP 706107	A1	19960410	EP 1995480139	A	19950922	199619 B
JP 8115295	A	19960507	JP 1995249814	A	19950927	199628 E
US 5548797	A	19960820	US 1994316976	A	19941003	199639 E
KR 163232	B1	19990115	KR 199533596	A	19950930	200037 E

Priority Applications (no., kind, date): US 1994316976 A 19941003

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
EP 706107	A1	EN	8	3	
Regional Designated States,Original: DE FR GB					
JP 8115295	A	JA	8		
US 5548797	A	EN	7	4	

...uses clock positioning circuit to position in time, signals generated from system clock and combined with other clock signals to generate single clock

Original Titles:
...INPUT-OUTPUT CONTROLLER AND SYSTEM FOR EXECUTING POSITIONING OF CLOCK SIGNAL OUTPUT...

...Digital clock pulse positioning circuit for delaying a signal input by a fist time duration and a second time duration to provide a positioned clock signal.

Alerting Abstract ...output controller (130) includes a storage array (210) for temporarily storing data, and multiple clocks to access or update the data. One or more array clock signals are generated from a system clock (170) combined with other clock signals to generate a

single clock signal which is positioned in time by a clock positioning circuit to accommodate circuit throughput delay variations, and effectively reduce hold time to zero...

...generated in I/O channel controllers (114,116,118) to produce one or more array clocking signals to access the storage array (210). The system clock (170) and other clocks are combined in a combinational logic circuit (174) to produce a single clocking signal input to an array positioning circuit (220...

...USE/ADVANTAGE - In multiple processor systems having multiple clock timing signals. Allows array address and enable signals maximum time to become stable. Storage arrays may be clocked at significantly higher frequencies, and arrays may...

Title Terms.../Index Terms/Additional Words: CLOCK;

Original Publication Data by Authority

Original Abstracts:
...input/output channel controller includes a storage array for temporarily storing data and multiple clocks to access or update the data. One or more array clock signals are generated from a system clock combined with other clock signals to generate a single clock signal which is positioned in time by a clock positioning circuit to accommodate circuit throughput delay variations and to effectively reduce hold time to zero. Storage arrays may be clocked at significantly higher frequencies and arrays may have...

...input/output channel controller includes a storage array for temporarily storing data and multiple clocks to access or update the data. One or more array clock signals are generated from a system clock combined with other clock signals to generate a single clock signal which is positioned in time by a clock positioning circuit to accommodate circuit throughput delay variations and to effectively reduce hold time to zero. Storage arrays may be clocked at significantly higher frequencies and arrays may have multiple gated clocks without incurring...
Claims:
...a system control unit; and</br> one or more input/output channel control units (IOCC), each of said IOCC units comprising a storage array, and a clock positioning circuit to position clock signals output from said clock positioning circuit to be active when information inputs to said array are stable...

...a system control unit;</br>one or more input/output channel control units (IOCC), each of said IOCC units comprising a storage array and a digital clock positioning circuit to position clock signals output from said digital clock pulse positioning circuit to be active when information inputs to said array are stable;</br>wherein said digital clock pulse positioning circuit further comprises:</br>a first digital delay circuit for delaying an input signal by a first time duration T1;</br>a second digital delay circuit responsive to an output of said first digital delay circuit for delaying a signal input to said second digital delay circuit by a second time duration T2; and</br>circuit means responsive to an output of said first digital delay circuit and an output of said second digital delay circuit for providing a positioned clock signal for said array. Basic Derwent Week: 199619

NPL Abstract Files

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File 256:TecInfoSource 82-2007/Aug(c) 2007 Info.Sources Inc
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec(c) 2006 The Thomson Corp
File 266:FEDRIP 2007/JunComp & dist by NTIS, Intl Copyright All Rights Res
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13(c) 2002 The Gale Group

Set Items Description
S1 30567 CLOCK (3N) (CYCLE? OR RATE?? ? OR SPEED? OR PULS??? OR CIR-
CUIT?)
S2 2505427 BACKUP? OR BACK??? () UP OR COPY OR COPIES OR COPYING OR -
COPIED OR REBUILD? OR REPLACING OR REPLACEMENT? OR RESTORE?
? OR RESTORING OR RESTORED OR UPDATE OR UPDATING OR UPDATED
S3 958890 SAVE OR SAVING OR SAVED OR STORE OR STORED OR STORING OR K-
EEP?
S4 84 S1 AND S2 (50N) S3
S5 37768807 TWO OR 2 OR MORE OR SOME OR MULTI OR MULTIPLE OR ANOTHER OR
DIFFERENT OR OTHER? ? OR ADDITIONAL? OR BOTH OR MANY OR ASSO-
RTED OR SEVERAL OR FEW OR SECOND OR DUPLICAT? OR DOUBL? OR DU-
AL OR ITERAT? OR PLURAL OR TWIN? ? OR TWINNED OR TWICE
S6 8576917 CHANG??? OR CONVERT? OR EXCHANG? OR REPLAC??? OR SUBSTITUT-
??? OR SWAP??? OR SWITCH???
S7 6397103 CONSECUTIVE? OR ENSUING OR FOLLOW???? OR SEQUENCE?? ? OR S-
EQUENTIAL? OR SUCCESSI?
S10 51127 S5 (5N) S6 (5N) S7
S11 17 S1 (10N) S10
S12 784803 LATENC? OR LULL?? OR PAUSE? ? OR WAIT? ? OR WAITING OR HI-
NDER?? OR HOLD???
S13 4743911 CONSTANT? OR STABILE OR STABLE OR STEADY OR UNBROKEN OR UN-
CHANG? OR UNFLUCTUAT? OR UNIFORM? OR UNINTERRUPT? OR UNVARY?
S14 12468 S12 (5N) S13
S15 6 S1 (5N) S14
S16 13 S1 (15N) S14
S17 38 S1 (20N) S2 (20N) S3
S18 61 S11 OR S15 OR S17
S19 34 S18 AND PY=1963:2002
S20 20 RD (unique items)

20/5/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

08736510 INSPEC Abstract Number: B2003-10-1265A-093, C2003-10-5210B-062

Title: Switching activity minimization by efficient instruction set architecture design

Author(s): Ramakrishna, V.; Kumar, R.; Basu, A.

Conference Title: 2002 45th Midwest Symposium on Circuits and Systems. Conference Proceedings (Cat. No.02CH37378) Part vol.2 p. II-485-8 vol.2

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2002 Country of Publication: USA 3 vol.(xlii+686+678+699) pp.

ISBN: 0 7803 7523 8 Material Identity Number: XX-2003-00383

U.S. Copyright Clearance Center Code: 0-7803-7523-8/02/$17.00

Conference Title: Midwest Symposium on Circuits and Systems

Conference Sponsor: IEEE Circuits & Syst. Soc.; School of Electr. & Comput. Eng. at Oklahoma State Univ

Conference Date: 4-7 Aug. 2002 Conference Location: Tulsa, OK, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Power consumption can be greatly minimized by reducing the bus signal transition activity (also called switching activity) in the control and data path circuit. Switching activity occurs due to the **switching** between **two** instructions (of the embedded software) on **successive clock cycles**. Our belief is that the binary encoding of instructions (machine code) plays a significant role in determining the amount of switching in a circuit. Thus, our aim is to realise a machine encoding of instructions of an ASIP such that for a given data path, it will minimize the average switching activity in the control path circuit of the ASIP and hence the total switching activity in the ASIP. Given the application-domain of the ASIP, we have used information theoretic techniques to arrive at an encoding of the op-code that minimizes redundancy and also the switching activity. We have compared our encoding of instruction op-codes with those obtained by other encoding techniques using a switching activity estimator designed by us. (16 Refs)

Subfile: B C

Descriptors: application specific integrated circuits; clocks; instruction sets; integrated circuit design; minimisation of switching nets ; VLSI

Identifiers: switching activity minimization; instruction set architecture design; bus signal transition activity; data path circuit; clock cycles; machine encoding; total switching activity; information theoretic techniques; redundancy

Class Codes: B1265A (Digital circuit design, modelling and testing); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); C5210B (Computer-aided logic design)

20/5/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

06795118 INSPEC Abstract Number: C9802-6150C-018

Title: Exploiting dead value information

Author(s): Martin, M.M.; Roth, A.; Fischer, C.N.

Author Affiliation: Dept. of Comput. Sci., Wisconsin Univ., Madison, WI, USA

Conference Title: Proceedings. Thirtieth Annual IEEE/ACM International Symposium on Microarchitecture (Cat. No.97TB100184) p.125-35

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 1997 Country of Publication: USA xiii+369 pp.

ISBN: 0 8186 7977 8 Material Identity Number: XX97-03004

U.S. Copyright Clearance Center Code: 1072-4451/97/$10.00

Conference Title: Proceedings of 30th Annual International Symposium on

Microarchitecture
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Microprogramming & Microarchit.; ACM Special Interest Group on Microarchit
Conference Date: 1-3 Dec. 1997 Conference Location: Research Triangle Park, NC, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: We describe dead value information (DVI) and introduce three new optimizations which exploit it. DVI provides assertions that certain register values are dead, meaning they will not be read before being overwritten. The processor can use DVI to track dead registers and dynamically eliminate unnecessary **save** and restore instructions from the execution stream at procedure calls and context switches. Our results indicate that dynamic saves and restore instances can be reduced by 46% for procedure calls and by 51% for context switches. In addition, **save**/**restore** elimination for procedure calls can improve overall performance by up to 5%. DVI also allows the processor to manage physical registers efficiently, reducing the size requirements of the physical register file. When the system **clock rate** as proportional to the register file cycle time, this optimization can improve performance. All of these optimizations can be supported with only a few new instructions and minimal additional hardware structures. (18 Refs)
Subfile: C
Descriptors: instruction sets; optimising compilers; parallel programming ; remote procedure calls; software performance evaluation; storage management
Identifiers: dead value information; optimizations; assertions; register values; dead registers; save instructions; restore instructions; procedure calls; context switches; performance; physical register file; system clock rate; register file cycle time; hardware structures
Class Codes: C6150C (Compilers, interpreters and other processors); C6110P (Parallel programming); C6150N (Distributed systems software)

20/5/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

06781398 INSPEC Abstract Number: B9801-1265B-123, C9801-5210B-092
Title: Micro-preemption synthesis: an enabling mechanism for multi-task VLSI systems
Author(s): Kim, K.; Karri, R.; Potkonjak, M.
Author Affiliation: Dept. of Electr. & Comput. Eng., Massachusetts Univ., Amherst, MA, USA
Conference Title: 1997 IEEE/ACM International Conference on Computer-Aided Design. Digest of Technical Papers (Cat. No.97CB36142) p. 33-8
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 1997 Country of Publication: USA xxvi+767 pp.
ISBN: 0 8186 8200 0 Material Identity Number: XX97-02917
U.S. Copyright Clearance Center Code: 1092-3152/97/$10.00
Conference Title: Proceedings of IEEE International Conference on Computer Aided Design (ICCAD)
Conference Sponsor: IEEE Circuits & Syst. Soc.; IEEE Comput. Soc.; ACM SIGDA; IEEE Electron Devices Soc
Conference Date: 9-13 Nov. 1997 Conference Location: San Jose, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: Task preemption is a critical enabling mechanism in multi-task

VLSI systems. On preemption, data in the register files must be preserved in order for the task to be resumed. This entails extra memory to save the context and additional clock cycles to restore the context. We present techniques and algorithms to incorporate micro-preemption constraints during multi-task VLSI system synthesis. Specifically, we have developed: algorithms to insert and refine preemption points in scheduled task graphs subject to preemption latency constraints; techniques to minimize the context switch overhead by considering the dedicated registers required to save the state of a task on preemption and the shared registers required to save the remaining values in the tasks; and a controller based scheme to preclude preemption related performance degradation. (16 Refs)

Subfile: B C

Descriptors: circuit optimisation; finite state machines; flow graphs; integrated circuit design; integrated logic circuits; logic CAD; minimisation; VLSI

Identifiers: micro-preemption synthesis; multi-task VLSI systems synthesis; task preemption; register files; clock cycles; preemption points ; scheduled task graphs; preemption latency constraint; context switch overhead minimization; registers; controller based scheme; performance degradation; logic CAD; finite state machines

Class Codes: B1265B (Logic circuits); B1130B (Computer-aided circuit analysis and design); B1265F (Microprocessors and microcomputers); B0260 (Optimisation techniques); B2570 (Semiconductor integrated circuits); C5210B (Computer-aided logic design); C7410D (Electronic engineering computing); C5120 (Logic and switching circuits); C1180 (Optimisation techniques)

20/5/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

06346908 INSPEC Abstract Number: B9609-6120B-075, C9609-5260-028

Title: Viterbi decoding with dual timescale traceback processing

Author(s): Joeressen, O.J.; Meyr, H.

Author Affiliation: Tech. Hochschule Aachen, Germany

Conference Title: Sixth IEEE International Symposium on Personal, Indoor and Mobile Radio Communications. PIMRC'95. Wireless: Merging onto the Information Superhighway (Cat. No.95TH8135) Part vol.1 p.213-17 vol.1

Publisher: IEEE, New York, NY, USA

Publication Date: 1995 Country of Publication: USA . 3 vol. (xxvii+xxiii+1389) pp.

ISBN: 0 7803 3002 1 Material Identity Number: XX95-01578

U.S. Copyright Clearance Center Code: 0 7803 3002 1/95/$4.00

Conference Title: Proceedings of 6th International Symposium on Personal, Indoor and Mobile Radio Communications

Conference Sponsor: Inf. Technol. Res. Centre; IEEE Commun. Soc.; IEEE; Telecommun. Res. Inst. Ontario; IEE; IEICE

Conference Date: 27-29 Sept. 1995 Conference Location: Toronto, Ont., Canada

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); New Developments (N); Practical (P)

Abstract: A new approach to traceback processing in Viterbi decoders is presented. The approach reduces memory requirements as compared to previous approaches by using different speeds during acquisition of the best trellis path and the subsequent decoding of a block of data. This dual timescale approach allows in-place updating of the stored information and matches the constraints of commodity semi-custom technologies, where (at the considered high dock rates) write accesses to a RAM usually require

more than one **clock cycle**. (17 Refs)
Subfile: B C
Descriptors: digital signal processing chips; random-access storage; Viterbi decoding; VLSI
Identifiers: Viterbi decoding; dual timescale traceback processing; memory reduction; trellis path; in-place updating; stored information; semicustom technologies; VLSI; RAM
Class Codes: B6120B (Codes); B1265F (Microprocessors and microcomputers); B2570 (Semiconductor integrated circuits); B1265D (Memory circuits); C5260 (Digital signal processing); C5135 (Digital signal processing chips); C5320G (Semiconductor storage)

20/5/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

05817614 INSPEC Abstract Number: B9412-1265F-042, C9412-5135-010
Title: A 3.84 GIPS integrated memory array processor LSI with 64 processing elements and 2 Mb SRAM
Author(s): Yamashita, N.; Kimura, T.; Fujita, Y.; Aimoto, Y.; Manabe, T.; Okazaki, S.; Nakamura, K.; Yamashina, M.
Author Affiliation: NEC Corp., Kawasaki, Japan
p.260-1
Editor(s): Wuorinen, J.H.
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA 400 pp.
ISBN: 0 7803 1844 7
U.S. Copyright Clearance Center Code: 0 7803 1844 7/94/$3.00
Conference Title: Proceedings of IEEE International Solid-State Circuits Conference - ISSCC '94
Conference Sponsor: IEEE Solid-State Circuits Council; IEEE Bay Area Council San Francisco Sect
Conference Date: 16-18 Feb. 1994 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P)
Abstract: An integrated memory array processor (IMAP) LSI has peak performance of 3.84 GIPS and is suitable for high-speed, low-level image processing (LIP). Keys to performance are: integration of 64 simple processing elements (PEs) and 2 Mb SRAM with 128 b I/O, and single-instruction stream multiple-data stream (SIMD) parallel processing by use of 1.28 GB/s on-chip processor-memory bandwidth. A large number of active sense amplifiers ordinarily used in a wide memory bandwidth creates the problem of large power consumption. The number of active sense amplifiers here is reduced by a factor of 4 by accessing half of each word at a time, but accessing it at twice the **speed** of the PE **clock**. This **keeps** power consumption low. Each memory block can perform indexed addressing within its pages. This capability contributes to IMAP flexibility and efficiency in LIP. To raise yield, the architecture employs 4-way block **replacement** redundancy. IMAP is fabricated in 0.55 mu m BiCMOS 2-layer metal process technology. (4 Refs)
Subfile: B C
Descriptors: BiCMOS integrated circuits; cellular arrays; digital signal processing chips; image processing equipment; large scale integration; parallel architectures; redundancy; SRAM chips
Identifiers: integrated memory array processor LSI; SRAM; high-speed image processing; low-level image processing; single-instruction stream multiple-data stream; SIMD parallel processing; onchip memory; active sense amplifiers; low power consumption; indexed addressing; 4-way block

replacement redundancy; BiCMOS IC; 2-layer metal process technology; DSP chip; 2 Mbit; 1.28 GB/s; 0.55 micron
Class Codes: B1265F (Microprocessors and microcomputers); B1265D (Memory circuits); B2570K (Mixed technology integrated circuits); B6140C (Optical information and image processing); C5135 (Digital signal processing chips) ; C5530 (Pattern recognition and computer vision equipment); C5220P (· Parallel architecture); C5320G (Semiconductor storage)
Numerical Indexing: storage capacity 2.1E+06 bit; byte rate 1.28E+09 Byte/s; size 5.5E-07 m

20/5/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

05070961 INSPEC Abstract Number: B9202-1265B-219, C9202-5230-063
Title: Bit-level systolic arrays for modular multiplication
Author(s): Koc, C.K.; Ching Yu Hung
Author Affiliation: Dept. of Electr. Eng., Houston Univ., TX, USA
Journal: Journal of VLSI Signal Processing vol.3, no.3 p.215-23
Publication Date: Sept. 1991 Country of Publication: Netherlands
CODEN: JVSPED ISSN: 0922-5773
U.S. Copyright Clearance Center Code: 0922-5773/91/$1.00+0.15
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: Presents bit-level cellular arrays implementing Blakley's (1983) algorithm for multiplication of two n-bit integers modulo another n-bit integer. The semi-systolic version uses 3n(n+3) single-bit carry save adders and 2n copies of 3-bit carry look-ahead logic, and computes a pair of binary numbers (C, S) in 3n clock cycles such that C+S in (0, 2N). The carry look-ahead logic is used to estimate the sign of the partial product, which is needed during the reduction process. The final result in the correct range (0, N) can easily be obtained by computing C+S and C+S-N, and selecting the latter if it is positive; otherwise, the former is selected. The authors construct a localized process dependence graph of this algorithm, and introduce a systolic array containing 3nw simple adder cells. The latency of the systolic array is 6n+w-2, where w=(n/2). The systolic version does not require broadcast and can be used to efficiently compute several modular multiplications in a pipelined fashion, producing a result in every clock cycle. (18 Refs)
Subfile: B C
Descriptors: digital arithmetic; systolic arrays
Identifiers: bit-level systolic arrays; pipeline processing; modular multiplication; bit-level cellular arrays; single-bit carry save adders; 3-bit carry look-ahead logic; binary numbers; clock cycles; partial product ; localized process dependence graph
Class Codes: B1265B (Logic circuits); C5230 (Digital arithmetic methods) ; C5120 (Logic and switching circuits)

20/5/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

04698796 INSPEC Abstract Number: B90054531, C90056983
Title: Carry-save adders for computing the product AB modulo N
Author(s): Koc, C.K.; Hung, C.Y.
Author Affiliation: Dept. of Electr. Eng., Houston Univ., TX, USA
Journal: Electronics Letters vol.26, no.13 p.899-900

Publication Date: 21 June 1990 Country of Publication: UK
CODEN: ELLEAK ISSN: 0013-5194
U.S. Copyright Clearance Center Code: 0013-5194/90/$3.00+0.00
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: The authors describe a new algorithm for modulator multiplication using carry-save adders. The proposed algorithm is based on the sign-estimation technique. A carry-save adder structure consisting of three rows of n+3 simple 1-bit adder cells, and two copies of 3-bit carry look-ahead logic can be used to implement a single step of the algorithm. A completely pipelined array for modular multiplication designed by cascading n carry-save adders performs modulator multiplication at the clock rate. (4 Refs)
Subfile: B C
Descriptors: adders; carry logic; digital arithmetic; multiplying circuits; pipeline processing
Identifiers: modulator multiplication; carry-save adders; sign-estimation technique; carry look-ahead logic; pipelined array
Class Codes: B1265B (Logic circuits); C5230 (Digital arithmetic methods) ; C5120 (Logic and switching circuits)

20/5/8 (Item 8 from file: 2)

DIALOG(R)File 2:INSPEC

04513613 INSPEC Abstract Number: C90001857
Title: BALLAST: a methodology for partial scan design
Author(s): Gupta, R.; Gupta, R.; Breuer, M.A.
Author Affiliation: Dept. of Electr. Eng.-Syst., Univ. of Southern California, Los Angeles, CA, USA
Conference Title: FTCS 19 Digest of Papers. The Nineteenth International Symposium on Fault-Tolerant Computing (Cat. No.89CH2754-0) p.118-25
Publisher: IEEE Comput. Soc. Press, Washington, DC, USA
Publication Date: 1989 Country of Publication: USA xxii+575 pp.
ISBN: 0 8186 1959 7
U.S. Copyright Clearance Center Code: 0731-3071/89/0000-0118401.00
Conference Sponsor: IEEE; Univ. Illinois at Urbana-Champaign; Univ. Iowa
Conference Date: 21-23 June 1989 Conference Location: Chicago, IL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Theoretical (T)
Abstract: In the proposed partial scan methodology, the scan path is constructed so that the rest of the circuit belongs to a class of circuits called balanced sequential structures. Test patterns for this structure are generated by treating it as being combinational. Each test pattern is applied to the circuit by shifting it into the scan path. holding it constant for a fixed number of clock cycles, loading the test result into the scan path, and then shifting it out. This technique achieves full coverage of all detectable faults with a minimal number of scannable storage elements and using only combinational test pattern generation. (12 Refs)
Subfile: C
Descriptors: graph theory; logic testing; sequential circuits
Identifiers: B-structures; design for testability; BALLAST; partial scan design; scan path; balanced sequential structures; detectable faults; combinational test pattern generation
Class Codes: C5210B (Computer-aided logic design); C1160 (Combinatorial mathematics)

20/5/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

04483409 INSPEC Abstract Number: B89068067
Title: A simple code converter for transmission over optical links
Author(s): Suvoroz, Ye.V.; Khaustov, A.I.
Journal: Radiotekhnika vol.42, no.11 p.27-8
Publication Date: Nov. 1987 Country of Publication: USSR
CODEN: RATEAO ISSN: 0033-8486
Translated in: Telecommunications and Radio Engineering, Part 2 (Radio Engineering) vol.42, no.11 p.61-2
Publication Date: Nov. 1987 Country of Publication: USA
CODEN: TCREAG ISSN: 0040-2508
U.S. Copyright Clearance Center Code: 0040-2508/87/0011-0061$7.50/0
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Digital data are not transmitted over optical communications links in the initial potential code, i.e., a 'nonreturn-to-zero' code (NRTZ) but rather by means of special linear codes. Specifically, 1B2B two-pulse codes are widely used, including a biphase code (BC) or, as it is called, the Manchester code. Timing diagrams are shown of a digital sequence in NRTZ and BC codes together with **clock pulses** (CP). There are **many** circuits that **convert** an initial digital **sequence** such as an NRTZ into a BC code and vice versa. The paper describes a comparatively simple design of a circuit for direct and reverse transformation of these codes. (2 Refs)
Subfile: B
Descriptors: code convertors; optical links
Identifiers: nonreturn to zero code; digital data; timing diagrams; code converter; optical links; linear codes; 1B2B two-pulse codes; biphase code; Manchester code; digital sequence; clock pulses; circuit
Class Codes: B1290B (Convertors); B6120B (Codes); B6260 (Optical links and equipment)

20/5/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

04095616 INSPEC Abstract Number: C88018161
Title: Fast triangularization by givens rotation using on line CORDIC
Author(s): Ercegovac, M.D.; Lang, T.
Issued by: Univ. California, Comput. Sci. Dept., Los Angeles, CA, USA
Publication Date: Sept. 1987 Country of Publication: USA 16 pp.
Report Number: CSD-870045
Language: English Document Type: Report (RP)
Treatment: Practical (P); Theoretical (T)
Abstract: A scheme for triangularization of a matrix using redundant and on-line CORDIC modules is proposed. Its implementation is simpler and faster than implementations using conventional CORDIC modules. The proposed scheme has the following features: the rotation processors use angles in a decomposed form thus eliminating the angle recurrence and allowing overlap between the angle processor and rotation processors: no ROMs are required; the (x,y)-recurrences are transformed so that only one variable shifter is required; the carry-propagate addition is replaced by a redundant addition (carry-**save** or signed-digit) thus reducing the **clock cycle**; the rotation recurrences are unfolded and implemented in on-line manner thus **replacing** the variable shifter with simple delays; the scale factor is computed in on-line manner; the scheme uses efficiently floating-point representations.

Subfile: C
Descriptors: digital arithmetic; modules; parallel processing
Identifiers: triangularization; matrix; on-line CORDIC modules; angle processor; rotation processors; rotation recurrences; scale factor; floating-point representations
Class Codes: C5230 (Digital arithmetic methods); C5440 (Multiprocessor systems and techniques)

20/5/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

03959537 INSPEC Abstract Number: C87053821
Title: Microprocessor-based multichannel transient recorder
Author(s): Joshi, P.N.; Mahalingam, V.; Renganathan, S.
Author Affiliation: Nat. Aeronaut. Lab., Bangalore, India
Journal: IEEE Transactions on Industrial Electronics vol.IE-34, no.2 p.148-52
Publication Date: May 1987 Country of Publication: USA
CODEN: ITIED6 ISSN: 0278-0046
U.S. Copyright Clearance Center Code: 0278-0046/87/0500-0148$01.00
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Data acquisition of fast time-varying phenomena relevant to structure dynamics and aerodynamic wind tunnel testing pose a number of problems such as speed, retrieval of data for analysis, number of channels, etc. To overcome these limitations, a software-based high-speed multichannel transient data acquisition system has been designed and developed. This system is built around the Burr-Brown SDM-853 Module. The data are **stored** in a 16-kbyte MOS RAM memory. The **stored** data are retrieved by a low-**speed** system **clock** through a digital-to-analog converter (DAC) onto an X-Y/t plotter for hard **copy**. (6 Refs)
Subfile: C
Descriptors: aerospace computing; computerised instrumentation; data acquisition; digital-analogue conversion; recorders
Identifiers: fast time-varying phenomena; structure dynamics; aerodynamic wind tunnel testing; software-based high-speed multichannel transient data acquisition system; Burr-Brown SDM-853 Module; 16-kbyte MOS RAM memory; low-speed system clock; digital-to-analog converter; X-Y/t plotter
Class Codes: C5520 (Data acquisition equipment and techniques); C7460 (Aerospace engineering)

20/5/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

03424950 INSPEC Abstract Number: B85022217
Title: Test oriented circuit design
Author(s): Thummel, D.
Author Affiliation: Iftest GmbH, Munchen, West Germany
Journal: Elektronik Industrie vol.15, no.9 p.15-18
Publication Date: 1984 Country of Publication: West Germany
CODEN: EKIDAT ISSN: 0374-3144
Language: German Document Type: Journal Paper (JP)
Treatment: General, Review (G)
Abstract: Many examples are given of bad and good circuit design from automatic testing point of view. Among discussed recommendations are: arrangement of test points in analogue and digital circuits; always using

identical circuits for identical purposes; using as much as possible identical functional blocks; separating analogue and digital circuitry; providing pull-up facilities for flip-flop switches and counters; direct control access to all **store** input lines; test facilities for feedback loops; provisions for **replacement** of internal **clock** by external **pulse** trains; provision of external means for the reduction of time scale in asynchronous circuits; **keeping** bridge and optional connections in connectors; and the use of pull-up resistors in tristate nodes. (0 Refs)
Subfile: B
Descriptors: automatic testing; electronic equipment testing; network synthesis
Identifiers: test oriented circuit design; analog circuitry; automatic testing; digital circuits; pull-up facilities; flip-flop switches; counters ; direct control access; store input lines; feedback loops; asynchronous circuits; pull-up resistors; tristate nodes
Class Codes: B0170E (Production facilities and engineering); B1130 (General analysis and synthesis methods)

20/5/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

03162666 INSPEC Abstract Number: B84003082
Title: Transistor tester: identification of correct connections of unknown devices
Author(s): Summ, P.
Journal: Funkschau no.17 p.83
Publication Date: 19 Aug. 1983 Country of Publication: West Germany
CODEN: FUSHA2 ISSN: 0016-2841
Language: German Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Describes a simple-to-use recognition instrument, with six LEDs indicating the six possible permutations of e, b, c leads. The instrument as such is far from simple, including no less than ten ICs and seven diodes, **two** **switches** and **some** passive components. The principle is that of automatic **sequential** probing, driven by a **clock**. Illustrations comprise the **circuit** diagram, components list and two printed board layout drawings. (0 Refs)
Subfile: B
Descriptors: bipolar transistors; semiconductor device testing; test equipment
Identifiers: transistor tester; connection identification; clock driver; recognition instrument; LEDs; ICs; diodes; switches; automatic sequential probing
Class Codes: B1290 (Special purpose electronic circuits); B7250G (Display, recording and indicating instruments)

20/5/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

02626205 INSPEC Abstract Number: B81008315
Title: Fluidic application of pseudonoise in dynamic characterization of instruments
Author(s): Updike, O.L.; McCallum, D.B.
Author Affiliation: Univ. of Virginia, Charlottesville, VA, USA
Journal: ISA Transactions vol.19, no.2 p.21-32
Publication Date: 1980 Country of Publication: USA

CODEN: ISATAZ ISSN: 0019-0578
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Pseudorandom test signals, applied with fluidic systems, offer advantages in determining the frequency response of fast systems such as biomedical instrumentation. Fluidic pseudonoise generators can supply inputs of concentration, flow, pressure, or temperature with a spectrum extending to hundreds of hertz. Two versions were tested. One, totally flueric, had adequate frequency range but was critical as to supply pressure, **clock pulses** for the shift register, loading, and general operating conditions. The **second** system generated pseudorandom **sequences** electronically, **converted** them to fluidic signals, and fluerically shaped the output. It performed well up to 50 Hz and, in characterization of a fast oxygen analyzer, yielded results consistent with earlier step tests. Amplitude characteristics agreed to approximately 40 Hz; and consistent phase data, previously unavailable, were measured to approximately 20 Hz. (11 Refs)
Subfile: B
Descriptors: biomedical equipment; frequency response; noise generators
Identifiers: fluidic systems; frequency response; fast systems; biomedical instrumentation; pseudorandom sequences; fast oxygen analyzer; fluidic pseudonoise generator; pseudorandom test signals; dynamic characterization
Class Codes: B7250E (Signal generators); B7510 (Biomedical measurement and imaging)

20/5/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

02361449 INSPEC Abstract Number: C79018201
Title: Fluidic application of pseudo-noise in dynamic characterization of instruments
Author(s): Updike, O.L.; McCallum, D.B.
Author Affiliation: Dept. of Biomedical & Chem. Engng., Univ. of Virginia, Charlottesville, VA, USA
Conference Title: 197 Joint Automatic Control Conference Part II p. 85-98
Publisher: ISA, Pittsburgh, PA, USA
Publication Date: 1978 Country of Publication: USA 416 pp.
Conference Sponsor: ISA; IEEE; et al
Conference Date: 15-20 Oct. 1978 Conference Location: Philadelphia, PA, USA
Language: English Document Type: Conference Paper (PA)
Abstract: Pseudo-random test signals, applied via fluidic systems, offer advantages in determining the frequency response of fast systems such as biomedical instrumentation. Fluidic pseudo-noise generators can supply inputs of concentration, flow, pressure, or temperature with a spectrum extending to hundreds of hertz. Two versions were tested. One, totally flueric, had adequate frequency range but was critical as to supply pressure, **clock pulses** for the shift register, loading, and general operating conditions. The **second** system generated pseudorandom **sequences** electronically, **converted** them to fluidic signals, and fluerically shaped the output. (11 Refs)
Subfile: C
Descriptors: chemical technology
Identifiers: instruments; fluidic systems; frequency response; biomedical instrumentation; concentration; flow; pressure; temperature; supply pressure; clock pulses; shift register; loading; pseudo noise; dynamic characterisation; chemical sensors

Class Codes: C3350G (Chemical and oil refining industries)

20/5/16 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06966774 E.I. No: EIP94111436646
Title: 3.84GIPS integrated memory array processor LSI with 64 processing elements and 3Mb SRAM
Author: Yamashita, Nobuyuki; Kimura, Tohru; Fujita, Yoshihiro; Aimoto, Yoshiharu; Manabe, Takashi; Okazaki, Shin'ichiro; Nakamura, Kazuyuki; Yamashina, Masakazu
Corporate Source: NEC Corp, Kawasaki, Jpn
Conference Title: Proceedings of the 1994 IEEE International Solid-State Circuits Conference
Conference Location: San Francisco, CA, USA Conference Date: 19940216-19940218
E.I. Conference No.: 20737
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1994. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 260-261
Publication Year: 1994
CODEN: DTPCDE ISBN: 0-7803-1845-5
Language: English
Document Type: CA; (Conference Article) Treatment: X; (Experimental); G ; (General Review); A; (Applications)
Journal Announcement: 9412W2
Abstract: An integrated memory array processor (IMAP) LSI has peak performance of 3.84GIPS and is suitable for high-speed, low-level image processing (LIP). Keys to performance are: integration of 64 simple processing elements (PEs) and 2Mb SRAM with 128b I/O, and single-instruction stream multiple-data stream (SIMD) parallel processing by use of 1.28GB/s on-chip processor-memory bandwidth. A large number of active sense amplifiers ordinarily used in a wide memory bandwidth creates the problem of large power consumption. The number of active sense amplifiers here is reduced by a factor of 4 by accessing half of each word at a time, but accessing it at twice the **speed** of the PE **clock**. This **keeps** power consumption low. Each memory block can perform indexed addressing within its pages. This capability contributes to IMAP flexibility and efficiency in LIP. To raise yield, the architecture employs 4-way block **replacement** redundancy. 4 Refs.
Descriptors: *Random access storage; Microprocessor chips; Arrays; Schematic diagrams; Fabrication; Image processing
Identifiers: Integrated memory array processor; Single instruction multiple data stream; Block replacement redundancy; High bandwidth systems; Static memory; SRAM
Classification Codes:
722.4 (Digital Computers & Systems); 714.2 (Semiconductor Devices & Integrated Circuits); 715.1 (Electronic Equipment, non-communication); 741.3 (Optical Devices & Systems); 723.2 (Data Processing)
722 (Computer Hardware); 714 (Electronic Components); 715 (General Electronic Equipment); 741 (Optics & Optical Devices); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS); 74 (OPTICAL TECHNOLOGY)

20/5/17 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04800723 E.I. Monthly No: EI8509083509 E.I. Yearly No: EI85104594
Title: PARALLEL PIPELINE MULTIPLIER IN A SIGNAL PROCESSOR.
Author: Anon
Source: IBM Technical Disclosure Bulletin v 28 n 2 Jul 1985 p 547-549
Publication Year: 1985
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 8509
Abstract: A parallel pipeline multiplier with enhanced performance and flexibility including extended precision operation and scaling control on input and output variables is described. Control is provided which permits the contents of the multiplier to be **saved** and **restored** when the processor is interrupted. Partial product and complete product registers operate simultaneously during each **clock cycle**. In the event of interrupt, the contents of both registers are **saved** and **restored**. This is a critical requirement for multipliers which employ pipelines operation to achieve throughput performance.
Descriptors: *SIGNAL PROCESSING--*Equipment
Identifiers: PARALLEL PIPELINE MULTIPLIER; SCALING CONTROL
Classification Codes:
716 (Radar, Radio & TV Electronic Equipment); 717 (Electro-Optical Communications); 718 (Telephone & Line Communications); 722 (Computer Hardware); 723 (Computer Software)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING)

20/5/18 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03520514 E.I. Monthly No: EI7603015534 E.I. Yearly No: EI76014130
Title: DELAY LINE IN SHIFT REGISTER SPEEDS M-SEQUENCE GENERATION.
Author: Harvey, J. T.
Corporate Source: Amalgamated Wireless Ltd, North Ryde, Aust
Source: Electronics v 48 n 24 Nov 27 1975 p 104-105
Publication Year: 1975
CODEN: ELECAD ISSN: 0013-5070
Language: ENGLISH
Journal Announcement: 7603
Abstract: The **clock rate** of a shift-register generator of maximal-length pulse **sequences** is significantly increased when a delay line **replaces** one or **more** of the register's stages. High-speed m-**sequences**, as maximal-length pulse sequences are called, are needed for testing data links, for generating repeatable pseudo-noise, and in spread-spectrum techniques. Repetitive sequences of pulses can be generated by connecting the output of a shift register back to the input in some way, setting in some initial condition that is not all zeroes, and turning on the clock. In this situation, the length of the repeating pulse sequence that emerges from the register depends upon the feedback arrangement and perhaps upon the initial condition. However, the m-sequence is independent of the starting condition. The limit to high-speed operation of this device occurs when the interval between clock pulses is less than the combined effective propagation delay in a shift-register stage and the exclusive -- OR gate. Provided that operation is required over a limited range of clock frequency, then the first stage of the shift register can be removed and a delay line substituted.
Descriptors: *COMPUTERS, DIGITAL--*Shift Registers
Classification Codes:
722 (Computer Hardware)

20/5/19 (Item 1 from file: 35)

01673489 ORDER NO: AAD99-09175

AUTOMATIC SYNTHESIS OF APPLICATION-SPECIFIC PROGRAMMABLE PROCESSORS (RECONFIGURABLE COMPUTATION, TASK PREEMPTION)

Author: KIM, KYOSUN

Degree: PH.D.
Year: 1998
Corporate Source/Institution: UNIVERSITY OF MASSACHUSETTS (0118)
Director: RAMESH KARRI
Source: VOLUME 59/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 5501. 127 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544

As witnessed by their recent rapid market growth, reconfigurable multi-functional data paths are an attractive alternative to both fully programmable and fully custom hardware platforms. We present a methodology for behavioral synthesis of an important and large class of reconfigurable data path designs, application specific programmable processors (ASPPs). ASPPs are data paths which provide efficient implementation for any of N functional specifications assuming that only one will be executed at any given time. The synthesis of ASPP designs imposes numerous new tasks on behavioral synthesis tools. We address bundling of applications, where n control-data flow graphs are bundled into at most m groups so that the area overhead is minimized, and all throughput constraints are satisfied. A variety of application specific constraints such as manufacturing cost minimization and risk reduction constraints are incorporated with application bundling.

Task preemption is a critical enabling mechanism in a variety of multi-task real-time application scenarios. On preemption, data in the register files must be preserved in order for the task to be resumed. This entails extra memory to preserve the context and additional clock cycles to save and restore the context. We propose techniques and algorithms to incorporate micro-preemption constraints during ASPP synthesis. Specifically, we develop a controller based scheme to preclude preemption related performance degradation, techniques to minimize the context switch overhead, and algorithms to insert and refine preemption points in scheduled task graphs subject to preemption latency constraints. This on-the-fly task preemption distinguishes ASPPs from other adaptive computing architectures.

Using the architectural flexibility provided by behavioral synthesis scheduling and resource allocation, we develop a novel approach for permanent fault-tolerance. This technique combines the behavioral synthesis-based flexibility provided by each of multiple functionalities with judicious application-to-faulty-unit assignment either to maximize the permanent fault-tolerance of such ASPPs (resource constrained fault-tolerant ASPP synthesis) or to guarantee that the ASPP remains operational in the presence of all possible k-unit faults (fault-tolerance constrained ASPP synthesis).

We demonstrate the effectiveness of the overall approach, the synthesis algorithms, and software implementations on a number of industrial-strength designs.

05336066
INTEL PLANS BLITZ OF LOW-POWER 80486 CHIPS FOR PORTABLES
US - INTEL PLANS LOW-POWER 80486 CHIPS FOR PORTABLES
Computergram International (CGI) 24 September 1992 p1
ISSN: 0268-716X

Intel plans to bring many of the power-saving features now available in its 80386SL microprocessors to a broad range of 80486 processors designed for use in portable personal computers, PC Week reports. On November 9, the company plans to kick off a lengthy 80486 product announcement schedule with the new 80486SL, a powerful **update** to the 80386SL with **clock speeds** of 25MHz and 33MHz. Over the next year and into 1994, the company plans to release several new 80486SX, 80486 and DX2 chips for portables in its efforts to obsolete the 80386 and **keep** the chip cloners on the hop. The parts will have a fully static design, which enables the motherboard to stop drawing power between keystrokes, and an input-ouput restart feature that turns peripherals off and on quickly. The chips are seen powering kit costing over USDlr2k.*

COMPANY: INTEL
PRODUCT: Microprocessors (3674MG);
EVENT: NEW PRODUCT EXTENSION (33);
COUNTRY: United States (1USA); NATO Countries (420); South East Asia Treaty Organisation (913);

NPL Full Text Files

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*File 624: Homeland Security & Defense and 9 Platt energy journals added
Please see HELP NEWS624 for more
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File 553:Wilson Bus. Absolute 1982-2007/May (c) 2007 The HW Wilson Co
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File 635:Business Dateline(R) 1985-2007/Jun 02 (c) 2007 ProQuest Info&Learning
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File 647:CMP Computer Fulltext 1988-2007/Aug W3 (c) 2007 CMP Media, LLC
File 674:Computer News Fulltext 1989-2006/Sep W1 (c) 2006 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2007/Jun 01 (c) 2007 Dialog
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File 613:PR Newswire 1999-2007/Jun 04 (c) 2007 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30 (c) 1999 PR Newswire Association Inc
File 370:Science 1996-1999/Jul W3 (c) 1999 AAAS
File 20:Dialog Global Reporter 1997-2007/Jun 04 (c) 2007 Dialog
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File 484:Periodical Abs Plustext 1986-2007/May W4 (c) 2007 ProQuest
File 634:San Jose Mercury Jun 1985-2007/Jun 01 (c) 2007 San Jose Mercury News

Set Items Description
S1 76528 CLOCK (3N) (CYCLE? OR RATE?? ? OR SPEED? OR PULS??? OR CIR-
CUIT?)
S2 13579952 BACKUP? OR BACK??? () UP OR COPY OR COPIES OR COPYING OR -
COPIED OR REBUILD? OR REPLACING OR REPLACEMENT? OR RESTORE??
OR RESTORING OR RESTORED OR UPDATE OR UPDATING OR UPDATED
S3 16874768 SAVE OR SAVING OR SAVED OR STORE OR STORED OR STORING OR K-
EEP?
S4 9321 S1 AND S2 AND S3
Limitall/s4
S5 9309 TWO OR 2 OR MORE OR SOME OR MULTI OR MULTIPLE OR ANOTHER OR
DIFFERENT OR OTHER? ? OR ADDITIONAL? OR BOTH OR MANY OR ASSO-
RTED OR SEVERAL OR FEW OR SECOND OR DUPLICAT? OR DOUBL? OR DU-
AL OR ITERAT? OR PLURAL OR TWIN? ? OR TWINNED OR TWICE
S6 8003 CHANG??? OR CONVERT? OR EXCHANG? OR REPLAC??? OR SUBSTITUT-
??? OR SWAP??? OR SWITCH???
S7 4857 CONSECUTIVE? OR ENSUING OR FOLLOW???? OR SEQUENCE?? ? OR S-
EQUENTIAL? OR SUCCESSI?
S8 193 S5 (5N) S6 (5N) S7
S9 5416 LATENC? OR LULL?? OR PAUSE? ? OR WAIT? ? OR WAITING OR HI-
NDER?? OR HOLD???
S10 2705 CONSTANT? OR STABILE OR STABLE OR STEADY OR UNBROKEN OR UN-
-CHANG? OR UNFLUCTUAT? OR UNIFORM? OR UNINTERRUPT? OR UNVARY?
S11 97 S9 (5N) S10
S12 971 (ACTIVE OR ACTIVAT??? OR CURRENT??? OR TOP OR FRONT OR FO-
CUS? OR SELECT???)(15N) WINDOW???
S13 7289 (REGISTER? OR MEMORY)
S14 64 S12 (10N) S13
S16 7 S8 AND S11

S26 7 CONSTANT (5N) LATENC?
S27 5 S26 AND PY=1963:2002
S37 47 (2 OR TWO) (3N) SWAP?
S38 44 S37 AND PY=1963:2002
S39 31 RD (unique items)

27/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01818050 SUPPLIER NUMBER: 17369140 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Real-world multimedia.(includes related articles on multimedia for Ethernet networks and on broadcast digital video technology)(Buyers Guide)
Gasiewski, Donna
DEC Professional, v14, n6, p20(6)
June, 1995
DOCUMENT TYPE: Buyers Guide ISSN: 0744-9216 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 3771 LINE COUNT: 00320

... voice and data for peer entities. You need a superior class of service to achieve this goal. This includes guaranteed bandwidth, delay and delay variation, **latency**, and **constant** reliability.
Interoperability with a WAN must also be provided for networked multimedia, or the system will be limited. IsoEthernet provides these features.
IsoEthernet provides the...

27/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01530956 SUPPLIER NUMBER: 12515725 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Scalability. (Ultracomputers: a Terflop Before its Time)
Communications of the ACM, v35, n8, p32(4)
August, 1992
ISSN: 0001-0782 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 5648 LINE COUNT: 00467

... messages to transfer data to other nodes. Build mechanisms to broadcast data and recombine results (TMC and Intel)
5. Multistream (or multithreaded), multiprocessors: Provide a **constant**, but long **latency** path between physical processors and memory. Build multi-instruction stream processors whereby one physical processor acts as many separate processors. Pre-fetch and post-store data to cover the long, **constant** **latency**. This processor can be used in all the preceding computers (Tera, T*, Alewife)
The Species
The specific distributed multicomputers of Figure 3 are segmented by

27/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01530955 SUPPLIER NUMBER: 12515571 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Ultracomputers: a teraflop before its time. (includes related article on Tera Taxonomy)

Bell, C. Gordon
Communications of the ACM, v35, n8, p26(22)
August, 1992
ISSN: 0001-0782 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 8984 LINE COUNT: 00747

... can issue multiple requests, a single physical processor appears to support 16 threads (or virtual processors). Thus, a processor appears to have access to a **constant**, zero **latency** memory. Since a processor is time-shared, it is comparatively slow and likely to be unusable for scalar tasks, and is hardly a general-purpose...

27/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01254690 SUPPLIER NUMBER: 07076175 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Bright lights, fast LANs. (Local Area Networks) (fiber optics)
Wu, Alan C.
PC Tech Journal, v6, n11, p96(11)
Nov, 1988
ISSN: 0738-0194 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 7462 LINE COUNT: 00601

... contract randomly as the signal travels around the ring. The cumulative effect of the jitter varies the bit latency of the ring. Unless the ring **latency** remains **constant**, bits are dropped as the **latency** decreases or are added as the latency increases. Timing jitter limits the number of stations in a ring.
To alleviate this problem, IEEE 802.5...

27/3,K/5 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)

00627563 92-42503
Ultracomputers: A Teraflop Before Its Time
Bell, Gordon
Communications of the ACM v35n8 PP: 26-47 Aug 1992
ISSN: 0001-0782 JRNL CODE: ACM
WORD COUNT: 13520

...TEXT: can issue multiple requests, a single physical processor appears to support 16 threads (or virtual processors). Thus, a processor appears to have access to a **constant**, zero **latency** memory. Since a processor is time-shared, it is comparatively slow and likely to be unusable for scalar tasks, and is hardly a general-purpose...messages to transfer data to other nodes. Build mechanisms to broadcast data and recombine results (TMC and Intel)

5. MULTISTREAM (OR MULTITHREADED), MULTIPROCESSORS: Provide a **constant**, but long **latency** path between physical processors and memory. Build multi-instruction stream processors whereby one physical processor acts as many separate processors, pre-fetch and post-store data to cover the long, **constant** **latency**. This processor can be used in all the preceding computers (Tera, T*, Alewife)
THE SPECIES

The specific distributed multicomputers of Figure 3 are segmented by...

26/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

03000829 SUPPLIER NUMBER: 149633927 (USE FORMAT 7 OR 9 FOR FULL TEXT
)
Designing Ethernet into industrial applications.
EDN, 51, 17, 57
August 17, 2006
ISSN: 0012-7515 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 2771 LINE COUNT: 00235

... constant and small forwarding delay that Table 1 shows is independent of packet size. Hence, fixing the size of the packets in a network provides **constant** switch **latency**. To reduce overall switch latency, you should minimize packet size.

To reduce latency jitter in the network, the EPL (Ethernet Powerlink Group) recommends using 100BaseTX...

39/3,K/12 (Item 12 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01427971 SUPPLIER NUMBER: 10588760 (USE FORMAT 7 OR 9 FOR FULL TEXT)
The i750 video processor: a total multimedia solution. (includes related article on implementation, performance and system cost of the i750 video processor) (technical)
Harney, Kevin; Keith, Mike; Lavelle, Gary; Ryan, Lawrence D.; Stark, Daniel J.
Communications of the ACM, v34, n4, p64(15)
April, 1991
DOCUMENT TYPE: technical ISSN: 0001-0782 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 7147 LINE COUNT: 00571

... execute faster and parallelism means that fewer instructions are required.

The dual-bus nature of PB permits elegant constructs such as the following instruction to **swap** the values in **two** registers: x = y,y = x;

Or, consider the "butterfly," a key component of Fast Fourier Transform and Fast Cosine Transform algorithms; two variables "x" and...

Inventor Search

Inventor Search Patent Files

```
  File   2:INSPEC 1898-2007/Sep W3
  File   6:NTIS 1964-2007/Oct W1
  File   8:Ei Compendex(R) 1884-2007/Sep W3
  File  34:SCISEARCH(R) CITED REF SCI 1990-2007/SEP W4
  File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
  File  35:Dissertation Abs Online 1861-2007/Jul
  File  65:Inside Conferences 1993-2007/Sep 28
  File  99:Wilson Appl. Sci & Tech Abs 1983-2007/Aug

      Set  Items  Description
      ---  -----  -----------

Set   Items Description
S1     1792 AU=(KANT, S? OR KANT S?) OR AU=(TAM, K? OR TAM K?)
S6    23952 CLOCK (3N) (CYCLE? OR RATE?? ? OR SPEED? OR PULS??? OR CIRCUIT? )
S7        1 S1 AND S6

 7/5/1     (Item 1 from file: 34)
DIALOG(R)File  34:SCISEARCH(R) CITED REF SCI
(c) 2007 THE THOMSON CORP. All rts. reserv.

10122829   Genuine Article#: 487TZ   Number of References: 6
Title: The first MAJC microprocessor: A dual CPU system-on-a-chip
Author(s): Kowalczyk A (REPRINT) ; Adler V; Amir C; Chiu F; Chng CP; De
    Lange WJ; Ge YF; Ghosh S; Hoang TC; Huang BQ; Kant S; Kao YS;
    Khieu C; Kumar S; Lee L; Liebermensch A; Liu X; Malur NG; Martin AA;
    Ngo H; Oh SH; Orginos I; Shih L; Sur B; Tremblay M; Tzeng A; Vo D;
    Zambare S; Zong J
Corporate Source: Sun Microsyst Inc,Palo Alto//CA/94303 (REPRINT); Sun
    Microsyst Inc,Palo Alto//CA/94303
Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, 2001, V36, N11 (NOV), P
    1609-1616
ISSN: 0018-9200   Publication date: 20011100
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST,
    NEW YORK, NY 10017-2394 USA
Language: English   Document Type: ARTICLE
Geographic Location: USA
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC
Abstract: The first implementation of MAJC architecture achieves high
    performance by using very long instruction word (VLIW), single
    instruction multiple data (SIMD), and chip multiprocessing. The chip
    integrates two processors, a memory controller, two high-speed parallel
    I/O interfaces, and a PCI controller. The chip, fabricated in a
    0.22-mum CMOS process with six layers of copper interconnect, contains
    13 million transistors and operates at 500 MHz. It is packaged in a
    624-pin ceramic column grid array using flip-chip assembly technology.
Descriptors--Author Keywords: clock distribution ; CMOS integrated
    circuits ; CMP ; computer architecture ; coupling noise ;
    flip-flops ; high-speed integrated circuits ; logic design ;
    microprocessors
Cited References:
    HEALD R, 2000, V35, P1526, IEEE J SOLID-ST CIRC
    KLASS F, 1999, V34, P712, IEEE J SOLID-ST CIRC
    KOWALCZYK A, 2001, P236, ISSCC 2001
    NORMOYLE K, 1995, PR3, P HOT INT AUG
    ROHRER N, 1998, P240, ISSCC
```

TREMBLAY M, 2000, V20, P12, IEEE MICRO

Inventor Search Patent Files

```
  File 347:JAPIO Dec 1976-2007
  File 348:EUROPEAN PATENTS 1978-2007
  File 349:PCT FULLTEXT 1979-2007
  File 350:Derwent WPIX 1963-2007

Set     Items   Description
S1        217   AU=(KANT, S? OR KANT S?) OR AU=(TAM, K? OR TAM K?)
S2     146866   CLOCK (3N) (CYCLE? OR RATE?? ? OR SPEED? OR PULS??? OR CIR-
             CUIT? )
S3          4   S1 AND S2
S4          4   IDPAT (sorted in duplicate/non-duplicate order)
S5          4   IDPAT (primary/non-duplicate records only)

 5/5,K/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2007 The Thomson Corporation. All rts. reserv.

0009368462  - Drawing available
WPI ACC NO: 1999-302125/199925
XRPX Acc No: N1999-226349
Dynamic to static signal converter in staticized flip-flop circuit
Patent Assignee: SUN MICROSYSTEMS INC  (SUNM)
Inventor: TAM K W
Patent Family (1 patents,  1 countries)
Patent                          Application
Number          Kind   Date     Number          Kind   Date     Update
US 5900759       A   19990504  US 1997883546    A  19970626  199925  B

Priority Applications (no., kind, date): US 1997883546  A  19970626

Patent Details
Number         Kind  Lan   Pg  Dwg  Filing Notes
US 5900759       A   EN    13    7

  Alerting Abstract US A
  NOVELTY - A pull down path shut-off transistor (MC2) is connected in
series between pull down transistor and ground and is closed during one
phase of clock signal and opened during another. An activation transistor
(MC4) receives clock signal delayed by delay circuit, is coupled between
output node and pull down transistor.
  DESCRIPTION - The activation transistor is closed during one phase of
delayed clock signal and open during other phase. Pull down transistor is
connected between output node and ground. The pull down transistor is
closed when input node is at precharge potential and open when at ground
potential. Pull-up transistor is coupled between source voltage and output
node. The pull-up transistor is closed, when input node is at ground
potential and open when at precharge potential.
  USE - In staticized flip-flop circuit .
  ADVANTAGE - Glitching of static output of staticized flop is minimized.
Crowbar current is reduced by using activation transistor.
  DESCRIPTION OF DRAWINGS - The figure shows example of dynamic to static
converter.
  MC2 Pull down path shut-off transistor
  MC4 Activation transistor


Claims:
```

...device and the ground, which is closed during each first phase of a clock signal and which is open during each second phase of the clock signal;a delay circuit which receives and delays the clock signal by a delay which is less than a clock period to obtain a delayed clock signal having first and second delayed phases which are delayed by said delay...

5/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01522876
LOW POWER READ SCHEME FOR MEMORY ARRAY STRUCTURES
NIEDRIGES LEISTUNGSLESESCHEMA FUR SPEICHERARRAYSTRUKTUREN
PROCEDE DE LECTURE A FAIBLE CONSOMMATION D'ENERGIE POUR STRUCTURES DE MATRICES MEMOIRES
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (2616592), 4150 Network Circle, Santa Clara, California 95054, (US), (Proprietor designated states: all)
INVENTOR:
KANT, Shree, 5533 Alvelias Drive, Union City, CA 94587, (US)
SINGH, Gajendra, P., 1045 West Washington Avenue, 9e, Sunnyvale, CA 94086, (US)
LEGAL REPRESENTATIVE:
Weihs, Bruno Konrad (94361), Cabinet Osha Liang 121, Avenue des Champs Elysees, 75008 Paris, (FR)
PATENT (CC, No, Kind, Date): EP 1382042 A2 040121 (Basic)
EP 1382042 B1 060322
WO 2002086901 021031
APPLICATION (CC, No, Date): EP 2002725621 020410; WO 2002US11421 020410
PRIORITY (CC, No, Date): US 837390 010418
DESIGNATED STATES: DE; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): G11C-005/02; G11C-011/412; G11C-011/404; G11C-005/00
INTERNATIONAL CLASSIFICATION (V8 + ATTRIBUTES):

...SPECIFICATION the CPU (22). Typically, requested data that is in L1 cache (26) or L2 cache (28) is available to the CPU (22) three or more clock cycles after cycle in which the CPU (22) made the data request. However, requested data that is in the register files is usually available to the CPU (22...

5/5,K/3 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01351705 **Image available**
HIGH-SPEED DIFFERENTIAL LOGIC BUFFER
TAMPON LOGIQUE DIFFERENTIEL HAUTE VITESSE
Patent Applicant/Assignee:
ANALOG DEVICES INC, One Technology Way, Norwood, MA 02062-9106, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
TAM Kimo Y F, 11 Brooks Road, Lincoln, MA 01773, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
SANDVOS Jay et al (agent), Bromberg & Sunstein LLP, 125 Summer Street, Boston, MA 02110-1618, US
Patent and Priority Information (Country, Number, Date):

Patent: WO 200633886 A1 20060330 (WO 0633886)
Application: WO 2005US32499 20050912 (PCT/WO US2005032499)
Priority Application: US 2004945323 20040920
English Abstract
A circuit for a high speed digital buffer has an active load circuit connected to an output of the digital buffer. The active load circuit loads the buffer output with an active inductance to reduce the RC time constant at the buffer output. The active load circuit may be based on two active devices connected to the buffer output so as to form a differential cascode circuit.
Detailed Description
... Figure 4 shows the circuit structure for an active load buffer according to one embodiment of the present invention. One specific application of such a **circuit** is as a **clock** buffer to drive a differential clock signal into multiple differential current mode latches representing a relatively high load. Input signals VIP and VIN are applied...

5/5,K/4 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00952745 **Image available**
LOW POWER READ SCHEME FOR MEMORY ARRAY STRUCTURES
PROCEDE DE LECTURE A FAIBLE CONSOMMATION D'ENERGIE POUR STRUCTURES DE MATRICES MEMOIRES
Patent Applicant/Assignee:
SUN MICROSYSTEMS INC, MS UPAL01-521, 901 San Antonio Road, Palo Alto, CA 94303, US, US (Residence), US (Nationality)
Inventor(s):
KANT Shree, 34307 Bodkin Terrace, Fremont, CA 94555, US,
SINGH Gajendra P, 1045 West Washington Avenue, #9e, Sunnyvale, CA 94086, US,
Legal Representative:
ROSENTHAL Alan D (et al) (agent), Rosenthal & Osha L.L.P., 1221 McKinney, Suite 2800, Houston, TX 77010, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200286901 A2-A3 20021031 (WO 0286901)
Application: WO 2002US11421 20020410 (PCT/WO US0211421)
Priority Application: US 2001837390 20010418
English Abstract
A method and apparatus for consuming low power when accessing data from a memory array is provided. Further, a method and apparatus for consuming low power when accessing data from a segmented bit line structure in a register file is provided by using transistors having progressively smaller widths as the storage cells or segments they are in get closer to an output of the segmented bit line structure. Further, a method and apparatus for consuming low power when accessing data from a differential bit line structure in a register file is provided by using transistors having progressively smaller widths as the storage cells they are in get closer to an output of the differential bit line structure. Further, a method and apparatus for consuming low power when accessing data from a segmented differential bit line structure in a register file is provided by using transistors having progressively smaller widths as the storage cells or segments they are in get closer to an output of the segmented differential bit line structure.

Detailed Description
... the CPU (22).

Typically, requested data that is in L1 cache (26) or L2 cache (28) is available to the CPU (22) three or more **clock cycles** after **cycle** in which the CPU (22) made the data request. However, requested data that is in the register files is usually available to the CPU (22...

Supplemental References

US 5355345 A	19941011	Fully scalable memory apparatus
US 4727370 A	19880223	Method and system for synchronous handshake generation
US 6035391 A	20000307	Floating point operation system which determines an exchange instruction and updates a reference table which maps logical registers to physical registers
US 4833468 A	19890523	Layered network